Multicore Embedded System Using Parallel Processing Technique

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Abstract: Parallel simulation is a technique to execute multiple tasks simultaneously. Parallel simulation has the potential to accelerate the execution of simulation applications.. In this paper a parallel simulation technique using simulink model is investigated for a simple applications. A comparison results shows that the proposed technique is reduce the execution time compared with the sequential simulation technique. Also the wallance multiplier operation is implemented to investigate the parallel processing technique using FPGA SPARTEN3. In proposed proposed architecture at the final stage parallel prefix adder and modified carry save adder are used to reduce the delay than existing one. This technique was implemented efficiently and its work effectively. The result shows this method reduces the delay.

Keywords—simulink module, Wallace Multipliers, Sklansky adder, Kogge-Stone adder. Parallel processing, pipelining.

I. INTRODUCTION

Today, most small-scale simulation applications are implemented using sequential techniques. As the problem size increases, however, sequential techniques may be unable to manage the time complexity of the processing applications adequately. Parallel processing has the potential to accelerate the execution of simulation applications. However, parallel processing may not be effective for every application. Since the implementation of parallel processing for an application is usually very expensive, it is required to investigate the performance of parallel processing for a particular application before re-implementing the technique.

The proposed parallel processing model using simulink investigates the simulation of three applications simultaneously. Simulation of a system may have several objectives including,(i)understanding behaviour of a system (ii) obtaining estimates of performance of a system (iii) guiding the selection of design parameters (iv) validation of a model. Simulation has been used in many areas including manufacturing lines, communication networks, computer system , VLSI design, design automation, air traffic and road traffic systems, among others. Two separate classes of methodologies, called continuous time and discrete time simulation have emerged over the years and are widely used for simulating complex system.

II. EXISTING METHOD

The Existing architecture, Conventional Wallace multiplier Carry propagating adder is used at the final stage to reduce the delay. High-speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems. The major speed limitation in any adder is in the production of carries. The final stage CPA constitutes a dominant component of the delay in the parallel multiplier. Signals from the multiplier partial products summation tree do not arrive at the final CPA at the same time. This is due to the fact that the number of partial-product bits is larger in the middle of the multiplier tree

III. SIMULINK MODEL

First the investigation of parable processing technique using simlulink model is presented to perform the following three tasks:

1. Speed control of DC motor
2. Boost converter
3. AC to DC converter.

The block diagram of proposed system is given below. It has three inputs for three tasks. Three inputs are 1. Speed in rpm for DC motor 2.Voltage for boost converter 3. Angle in degrees. The given inputs are processed by corresponding module.

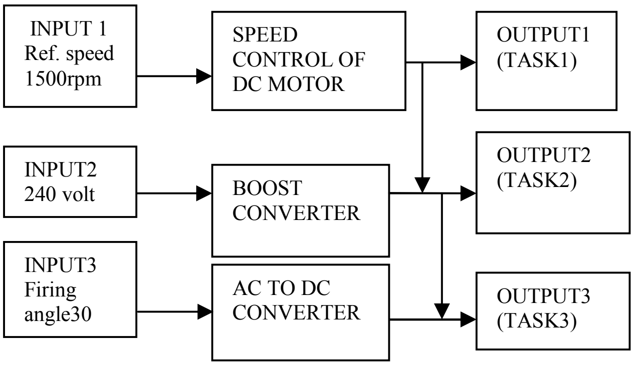

Fig1: Block diagram of Parallel simulation

Three tasks are running simultaneously. The first task controls the speed of the DC motor. The second task has an input of 240 V by which it boosts the speed of the DC motor. The third task converts AC signal to DC using a Thyristor. For every task a separate module is implemented and simulated.

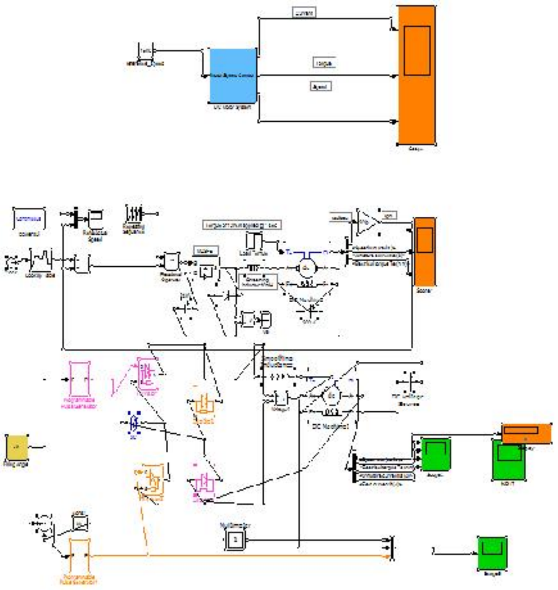

Fig: 2 Simulink Module

A. Speed control of DC motor

The figure 3 shows the simulation result and its executing the torque, current, speed of DC motor simultaneously, also its shows speed increase linearly.

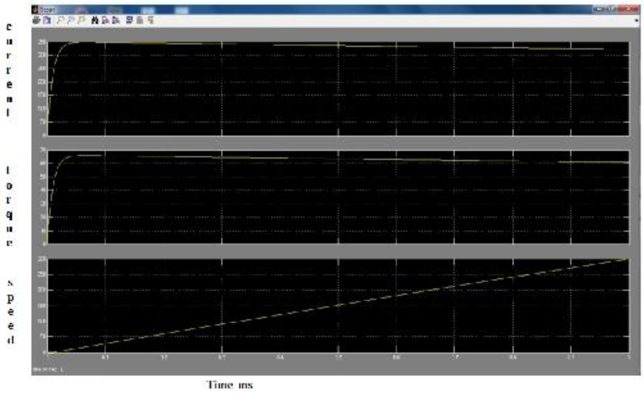

Fig 3: Simulation results for speed controls of the DC motor

The time versus current, speed and torque. The operation generated and it takes execution time of 0.007ms.to reach maximum of current 350amps, torque 65Nm, speed 290 rad/s.

B. Boost converter of DC motor

The figure 4 shows the simulation result of boost converter. The result shows, the time versus current, speed and torque.

The operation generated and it takes execution time of 0.972ms.to reach maximum of current 1000amps, torque 10-20 Nm, speed 10-20 rad/s. The value of constant time period is 0.5ms

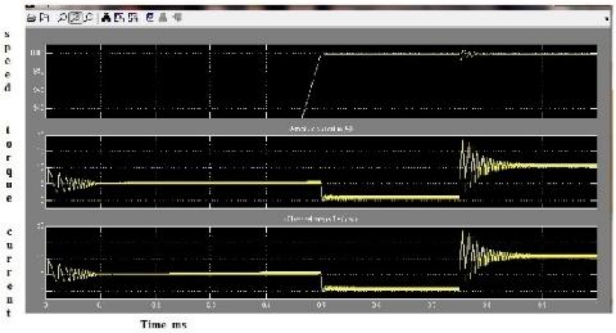

Fig 4: Simulation results for Boost converter of DC motor

C. AC to DC Converter

The figure 5 shows the simulation result of AC to DC converter.

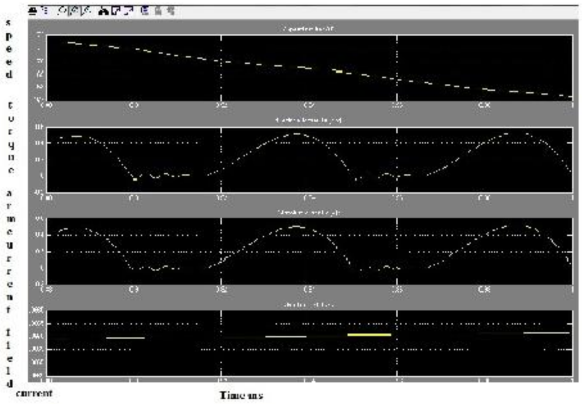

Fig 5: Simulation results for AC to DC converter of PWM

The result shows, the time versus current, speed and torque. The operation generated and it takes execution time of 0.975ms. to reach Maximum of current 0.4 amps, field current 1.065 amps torque 0.4 Nm, speed 171 rad/s. The proposed parallel simulation takes the average executing time is 0.998 ms for the three tasks.

(1)Speed control of DC motor

(2)Boost converter

(3) AC to DC Converter.

IV. COMPARISON RESULTS

Speed control of DC motor				
S.NO	PARAMETER	MAX VALUE (UNIT)	Sequential Execution Time	Parallel execution Time
1	Current(A)	3.5	0.007 ms	
2	Torque(Nm)	65		
3	Speed(rad/s)	290		
Boost converter				
1	Current(A)	10		

2	Torque(Nm)	10-20	0.972 ms	0.998 ms
3	Speed(rad/s)	10-20		
AC to DC Converter				
1	Speed(rad/s)	171	0.975ms	
2	Torque(Nm)	0.4		
3	Armature current(A)	0.4		
4	Field current(A)	1.065		

Table1: Result for Parallel simulation technique.

V. PROPOSED HARDWARE IMPLEMENTATION:

This paper proposes implementation of Wallace multipliers [5-6][Normal & Reduced Complexity] with reduced delay using parallel prefix adders at the final stage. Wallace multipliers perform in parallel, resulting in high speed. It uses full adders and half adders in their reduction phase. Reduced Complexity Wallace multiplier will have fewer adders than normal Wallace multiplier. In both multipliers, at the final stage, Carry propagating adder is used, which contributes to delay. This paper proposes, employing parallel prefix adders (fast adders) at the final stage of Wallace multipliers to reduce the delay.

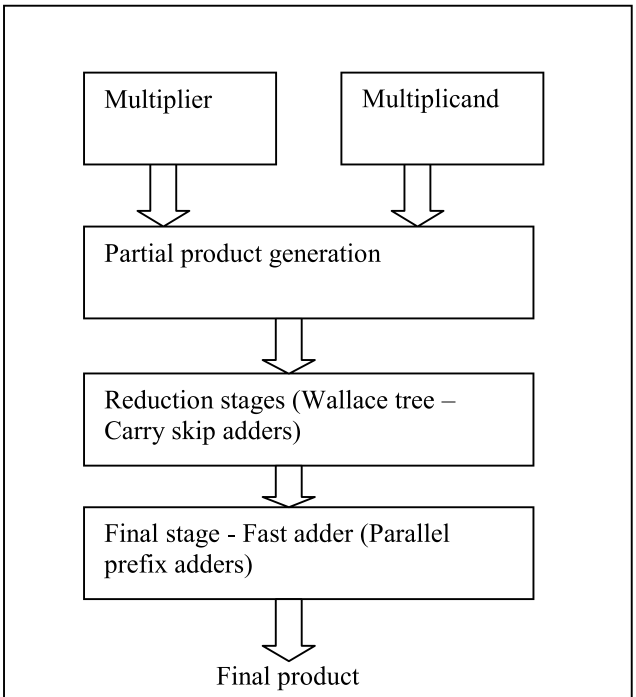
Multiplier
Multiplicand
Partial product generation
Reduction stages (Wallace tree – Carry skip adders)
Final stage - Fast adder (Parallel prefix adders)
Final product

Fig .6 Proposed Multiplier structure

VI. REDUCED COMPLEXITY WALLACE MULTIPLIER

This proposed method, which is the modified version of Wallace multiplier. It has less half adders than the normal Wallace multiplier. The partial products are formed by N2 AND gates. Reduced complexity Wallace multiplier diagram is shown below inFig.7.

The partial products are arranged in an “inverted triangle” order. The modified Wallace reduction method divides the matrix into three row groups.

1) Use full adders for each group of three bits in a column like the conventional Wallace reduction.

2) A group of two bits in a column is not processed, that is, it is passed on to the next stage (in contrast to conventional method). Single bits are passed on to the next stage as in the conventional Wallace reduction.

3) The only time half adders are used is to ensure that the number of stages does not exceed that of a conventional Wallace multiplier. For some cases, half adders are only used in the final stage of reduction.

In this Reduced complexity Wallace multiplier, at the final stage parallel prefix adder is used to reduce the delay.

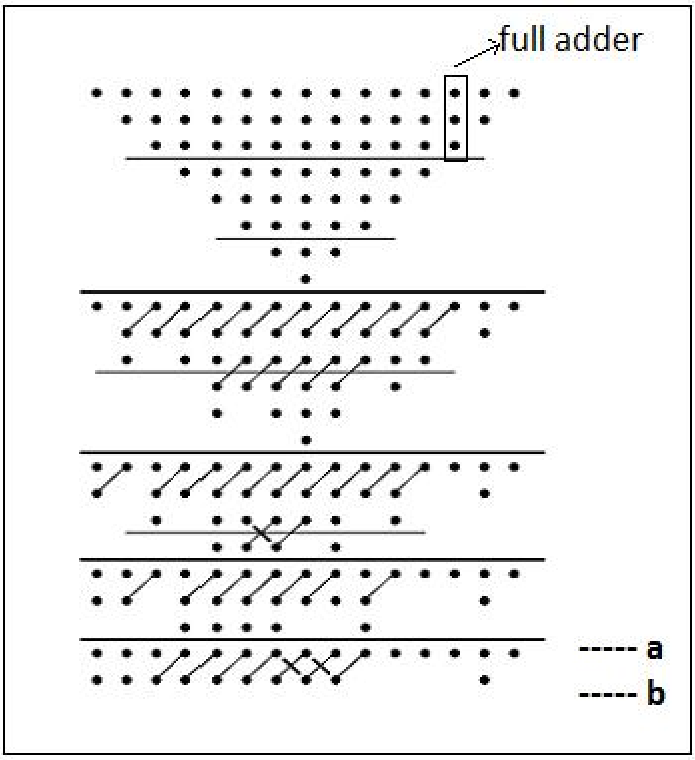

Fig.7 Reduced complexity Wallace multiplier

Parallel Prefix Adder

The Parallel prefix adder employs the three stage structure of the CLA adder. The improvement is in the carry generation stage, which is most intensive. Parallel prefix adder stage is shown in fig.8. Generally, the worst-case delay of the RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which is approximated by: where tc is the delay through the carry stage of a full adder, and ts is the delay to compute the sum of the last stage

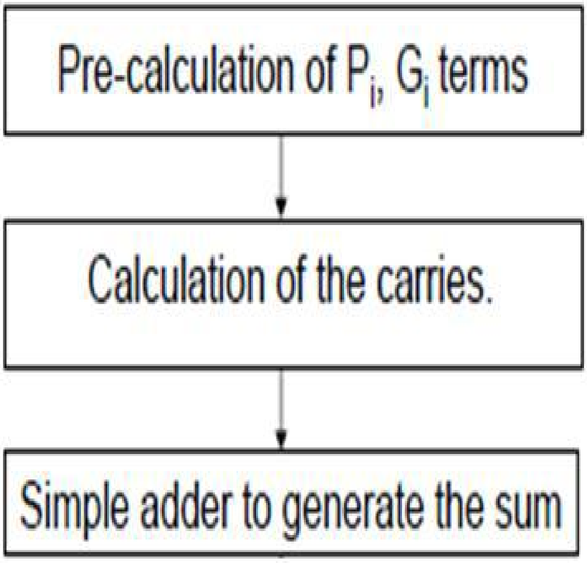
Pre-calculation of P$_i$, G$_i$ terms
Calculation of the carries.
Simple adder to generate the sum

Fig.8 Parallel Prefix Adder

The delay of ripple carry adder is linearly proportional to n, the number of bits. Therefore the performance of the RCA is limited when n grows bigger. The advantages of the RCA are lower power consumption as well as a compact layout giving smaller chip area. To design a larger adder ripple carry adders are cascaded. As of today standards, it is a common philosophy that area can be traded off in order to achieve higher speed.

Three Stages of Parallel Prefix Adder

Stage 1: Propagation, Generation terms & Partial sum:

$p (i) = a (i) \wedge b (i)$

$g (i) = a (i) \cdot g (i)$

$psum (i) = a (i) \wedge b (i)$

Stage 2: Prefix computation (Carry generation stage):

$P [i: j] = P [i: k] \cdot P [k\text{-}1: j]$, if $n \geq I > j \geq 1$

$G [i: j] = G [i: k] + (P [i: k] \cdot G [k\text{-}1: j])$, if $n \geq I > j \geq 1$

Where n = no. of bits

Stage 3: Final stage (sum & carry):

$c (i) = G [i:1]$

$Sum (i) = psum (i) \wedge c (i\text{-}1)$

VII. COMPARISON RESULTS

Multipliers	Number of delay (nano sec)	Number of slices
Wallace multipliers with skalansky adder	26.055 ns	86
Wallace multipliers with kogge stone adder	22.523 ns	96
Reduced complexity of Wallace multipliers	17.220 ns	97

Table.2 Result for Wallace Multipliers

VIII. CONCLUSION

The parallel simulation of simple application executed simultaneously using SIMULINK model. The task are (1) speed control of the DC motor,(2)Boost converter of DC motor and (3) AC to DC converter of PWM signal. After executing, the execution time of each task is measured using sequential technique and parallel simulation technique, finally comparison made for both the operations. The sequential simulation takes the average time of 1.944 units. But the Parallel simulation model takes the average time of 0.998 units for three tasks. This simulation technique reduces the time of 0.956 units. It proves parallel simulation technique takes less average execution time than sequential operation. Al so the parallel processing operation implemented using FPGA. Wallace multipliers using Parallel prefix adders at the final stage was implemented efficiently. From the results, it can be inferred that the proposed multipliers has lesser delay than the conventional multipliers. In processes, where repeated multiplication is done, this multiplier will provide significant performance. In future work is various applications are used for these multipliers of modified carry save adder.

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