RCEAT for RFID using Fast Search Algorithm

Pratyusha.pushadapu, Kavitha Jagabathuni and N L Vamsi Priya K

Abstract : **This paper presents a low power implementation of a secure EPC UHF passive digital base band processor designed for UWB transceiver on RFID for wireless application is described. To ensure the secure information transaction of the passive tag, traditionally the focus is on directly applying a low complexity encryption engine. The attackers could make use of known header to reveal the secret key. The proposed architecture consists of a novel clock and data flow solution enforced by an anti-collision algorithm engine embedded inside the RFID passive tag. Low power design techniques such as clock gating, optimal clock driving and parallel operation are extensively used in the design of the tag. The complete digital baseband processor RFID tag consists of a receive and transmit buffer a controller unit to control the data and clock, slot and reset counter ,random generator, comparator and memory controller. Increased power consumption, is one of the important factors, which governs the performance of the ICs in Ultra Deep Sub Micron (UDSM) regime. The hardware model of the complete digital baseband processor is modeled using verilog HDL code. The power optimization techniques such as clock gating, clock controlling was carried out for both transmitter and receiver sections operating at different frequencies.**

1. Introduction

RFID (Radio-Frequency Identification) technology has drawn a swirl of attention in the past few years as it helps identify objects and people in a fast, accurate and Inexpensive way. It has been applied into many areas, including passports, transportation payment, product tracing, automotive as well as animal identification etc. Nowadays the applications of RFID are increasing rapidly, including supply chain management, access control to buildings, public transportation, open-air events, airport baggage, and so on. To meet the market requirements, the preferred RFID system must exhibit features like low cost, long operation range and high data rate, requiring a small and low-voltage/low-power integrated Today, RFID is used in enterprise supply chain management to improve the efficiency of inventory tracking and management. However, growth and adoption in the enterprise supply chain market is limited because current commercial technology does not link the indoor tracking to the overall end-to-end supply chain visibility. Coupled with fair cost-sharing mechanisms, rational motives and justified returns from RFID technology investments are the key ingredients to achieve long-term and sustainable RFID technology adoption

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2. Methodology

In our proposed RCEAT the frame consists of slots and each slot (column) is divided into four minislots (rows). Therefore in each slot, four tags are allowed for contending the mini slots. The RCEAT will identify these four tags using the proposed Lookup table. The uniqueness of this proposed technique is reducing the tag identification time in the Binary Tree. The existing tags are divided into four in each Read cycle to reduce the required iterations and thus faster the tag identification. This proposed technique does not require the tag to remember the instructions from the reader during the identification process. Thus the tag is treated as an address carrying device only and memory-less tag can be designed which requires very low power. The RCEAT identification methodology is shown in Fig. 1. In RCEAT, bidirectional communications are involved, from the reader to the tag (Downlink) and from the tag to the reader (Uplink). When the reader detects there are tags exist in its interrogation zone, it will power these tags. Then the reader sends the Select-group command based on the tag Prefix or Object Class (OC). The selected tags group will move to the Ready state. Next the Reader transmits Reset signals and its frame. After that the frame is transmitted back to the reader, column by column starting with the first column. This compensates the time required for transmitting the packet to the reader. Therefore for every Read cycle, there are always available packets at the reader waiting for identification.

At the reader, the incoming packets for each link sequentially enter the RCEAT system. To avoid the four incoming packets from colliding with each other, these packets (IDs) are identified using the Binary Tree based technique with maximum four leaves. The reader selects these IDs using the proposed Fast-search Lookup table, and then the selected ID will be identified. Based on this proposed Lookup table, the four IDs will be identified from the smallest value to the largest one in one Read cycle. Then the tag that has successfully identified will be acknowledged by sending the Kill-tag.

3. Architecture

The RCEAT architecture consists of two subsystem; PreRCEAT and PostRCEAT In the PreRCEAT, the received messages are fed into the CRC-remover module. These received messages will be separated into two; the received packet and the received CRC.These packet and CRC are sent to the CRC- checker module for verification process.The CRC- checker module recalculated the CRC of the received packet. Then, this calculated CRC is compared with the received CRC. Otherwise or there are errors in the packet, the status-bit is set to two. After that, this updated status-bit is appended to its respective packet. The Status-

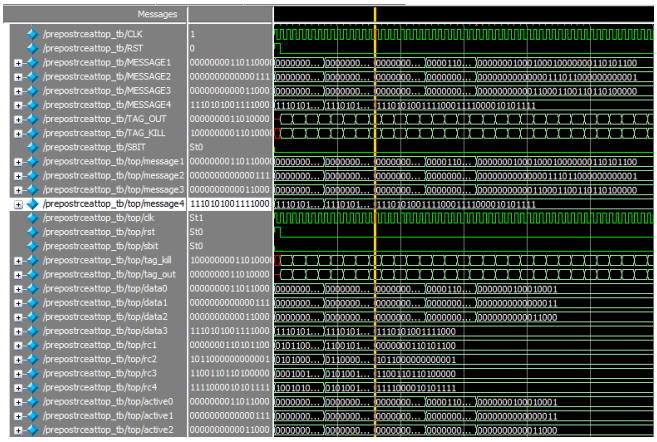
checker module will check any errors in the incoming packets. If there are errors, then reset the slot of the respective packet to zero value.

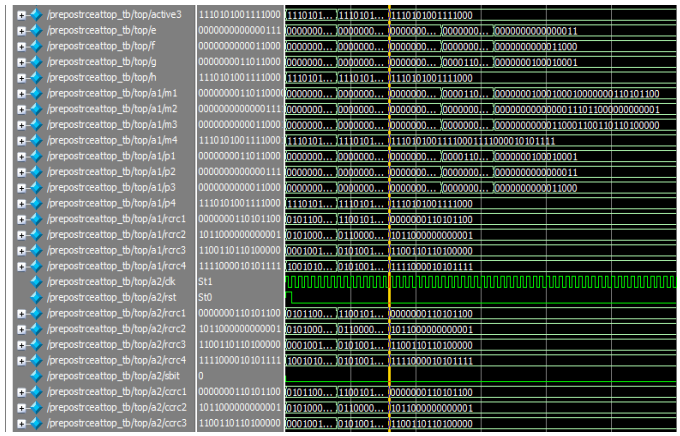
Otherwise, fill the slot of the packet with its respective ID. The status-bit is removed from its packet and only the tag's ID will be output to the PostRCEAT the active tags are divided into a group of four for every Read cycle in order to reduce the number of iterations in the identification process. The PostRCEAT reads all the ID bits at once regardless of its length. This is performed by using the word-byword multiplexing. During the identification process, the Fast-search module identifies the four tag's IDs simultaneously in one Read cycle which equal to a Tag clock cycle. The module firstly identifies the smallest ID bits until the largest one follows the Binary Tree with a maximum number of four leaves

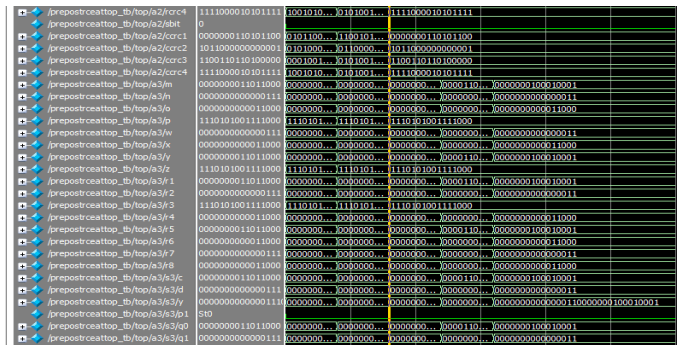
4. Simulation results

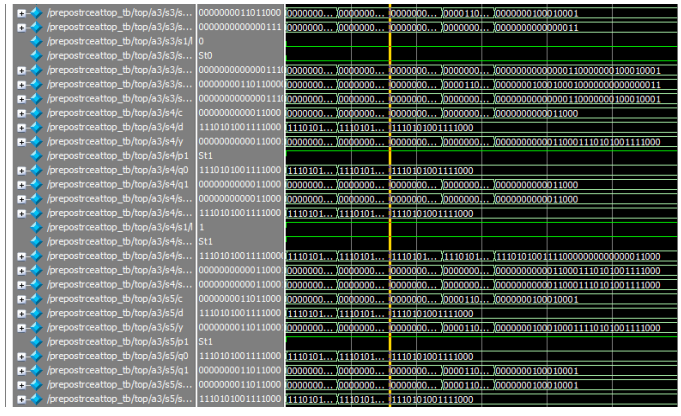
Verilog HDL codes for the RCEAT architecture have been successfully simulated and verified using the ModelSim XE II/Starter 5.7g tool. The following will discuss the Behavioral simulation waveforms for the selected ports in the RCEAT system as shown in Fig. 2. At the first Read cycle, for the received messages of $000C8584_{16}$, $0000550A5_{16}$, 000101231_{16}, and $0EA6093DF_{16}$, the recalculated CRC of these messages are 5844_{16}, $50A5_{16}$, 1231_{16}, and $93DF_{16}$ respectively. Asa result, the calculated CRCs are equal to the receivedCRCs which are represented by the four bit of the least significant bit (LSB) of the messages. Since there are no errors in the received messages, the Status-bit of the packets are set to zero, which are represented by the MSB of the packets; $000C8_{16}$, 00005_{16}, 00010_{16} and$0EA60_{16}$ respectively. Finally, the ID of these packets will be fed simultaneously to the PostRCEAT subsystem.

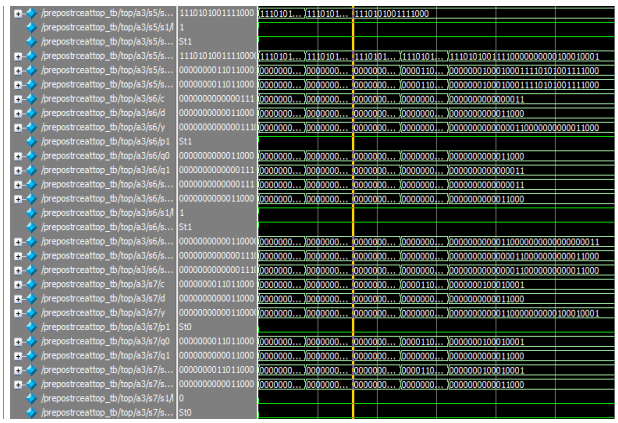
In the PostRCEAT subsystem, the Fast-search module will identify the four active tags simultaneously starting from the smallest value to the largest one. For examples, for the four input tag's ID of $00C8_{16}$, 0005_{16}, 0010_{16} and $EA60_{16}$ will be identified as 0005_{16}, 0010_{16},$00C8_{16}$ and $EA60_{16}$ respectively. Then these identified tags will be fed to the Read-kill tagmodule simultaneously at the negative edge of the Tag clock. Finally, the Read-killtag Module will output the four identified tags serially, one tag at every cycle of the system clock starting from the smallest tag's ID to the largest one. Moreover, at the same clock cycle, the identified tag will be killed.The RCEAT architecture has been implemented inhardware using the Field Programmable Grid Array (FPGA) model Virtex II Xc2v250. The output waveforms from the FPGA have been displayed using the Tektronix Logic Analyzer model TLA 5201 for real time verification. From the result, it shows that the system still enables to identify the tags without errors at the operating frequency of 180 MHz. Fig. 3 shows the FPGA output and its equivalent place and route simulation result at this frequency. For examples for the first Read cycle the identified tags are $03E5_{16}$, $0F90_{16}$,$18E0_{16}$ and $1FC8_{16}$ as marked by a circle.

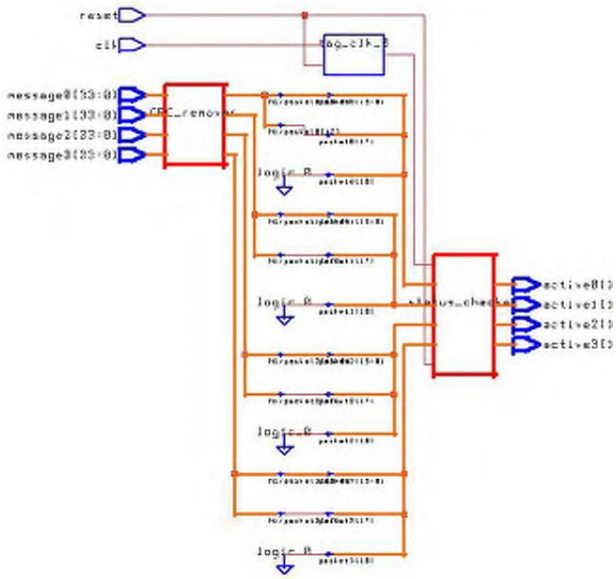




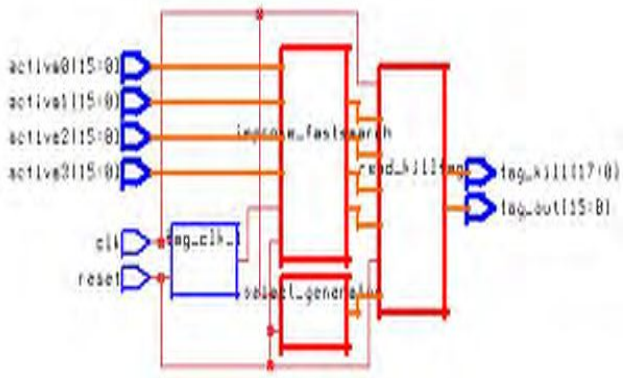








(a) PreRCEAT block diagram



(b) PostRCEAT block diagram

Fig. 4: Synthesized block diagram of RCEAT

The RCEAT system has been successfully implemented in hardware using FPGA with desired performances. Then the system is implemented on chip using ASIC approach. In this approach the system is resynthesized using 0.18µm Library, Synopsys Compiler and tools. Table 1 shows the output parameters using two synthesis technology; Xilinix and ASIC.

From the synthesis results, it shows the RCEAT architecture has the maximum operating frequency of 253 MHz and the total gates of 6,041. The average connection delay is 1.18 ns and the maximum pin delay is 5.35 ns. Moreover, the RCEAT occupies 0.03753 mm^2 cell area and consumes 7.578 mW powers. The data required time and the data arrival time are 2.72 ns and 2.31ns respectively.

Xilinx Parameters	**ASIC Parameters**
Max. Frequency=253MHz	Cell area= 0.03753 mm^2
Total gate count=6041	Power = 7.578 mW
Connection Delay=1.18ns	Arrival time=2.31ns
Max. pin Delay=5.35ns	Slack = 0.41 ns

Table 1 Synthesis result parameters

5. Conclusions

A proposed Reliable and Cost Effective Anti-collision technique (RCEAT) is designed to achieve a reliable and cost effective identification technique of the tag. The RCEAT architecture consists of two main subsystems; PreRCEAT checks error in the incoming packets using the CRC scheme. PostRCEAT identifies the error free packets using Binary Tree based technique. The architecture has been synthesized using Xilinix Synthesis Technology (XST). The RCEAT architecture also has been successfully implemented in hardware using FPGA model Virtex II Xc2v250. The FPGA outputs have been verified in real time using Tektronix Logic Analyzer model TLA 520. Finally on chip verification has been done using 0.18 µm Silterra Library, Synopsys Compiler and tools. The result shows that the architecture has smaller cell area, power consumption and number of gates. Therefore minimize the implementation and operating costs.

References

[1]. Yuechao Niu, Majid Baghaei Nejad, Hannu Tenhunen and Li-Rong Zheng, "*Design of a Digital Baseband Processor for UWB Tranceiver on RFID Tag*", IEEE Conference on Advanced Information Networking and Applications Workshop proceedings, vol. 2, pp. 358-361, May 2007

[2]. Adam S.W. Man, Edward S. Zhang, H.T. Chan, Vincent K.N. Lau, C.Y. Tsui and Howard C. Luong, "*Design and Implementation of a Low-power Baseband-system for RFID Tag"* IEEE International Solid-State Circuits Conference, pp. 1585-1588, May 2007

[3]. Usami M, Tanabe H, Sato A, Sakama I, Maki Y, Iwamatsu T, Ipposhi T and Inoue Y, "*A 0.05×0.05mm2 RFID Chip*

with Easily Scaled-Down ID-Memory", IEEE International Solid-State Circuits Conference, pp. 482-483, February 2007

[4]. He Yan, Hu Jianyun,Li Qiang and Min Hao, "*Design of Low-power Baseband processor for RFID Tag*", Proceedings of the IEEE International Symposium on Applications and the Internet Workshops, vol. 1, pp. 1-4, January 2006

[5]. He Yan, Hu Jianyun,Li Qiang and Min Hao, "*Design of Low-power Baseband processor for UHF RFID Tag*", 6th International Conference On ASIC, ASICON 2005, vol. 1, pp. 143-146, October 2005

[6]. Usami M, "*An Ultra Small RFID chip*", IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2004, pp. 241-244, June 2004

[7]. Masui S, Ishii E, Iwawaki T, Sugawara Y and Sawada K, "*A 13.56 MHz CMOS RF identification transponder integrated circuit with a dedicated CPU*", IEEE International Solid-State Circuits Conference, pp. 162-163, May 1999

[8]. Howes R, Williams A and Evans M, "*A read/write RFID tag for low cost applications*", IEE Colloquium on RFID Technology (Ref. No. 1999/123), pp. 4/1 - 4/4, February 1999

[9]. Yan HE, Jianyun HU and Hao MIN, "*An Ultra Low voltage, low power baseband-processor for UHF RFID tag*", Front. Electr. Electron. Eng China, Higher Education Press and Springer- Verlag, pp. 99-104, 2008

[10]. Jae-Hyung Lee, Ji-Hong Kim, Gyu-Ho Lim, Tae-Hoon Kim, Jung-Hwan Lee,Kyung-Hwan Park, Mu-Hun Park, Pan-Bong Ha, and Young-Hee Kim, *"Low-Power 512-Bit EEPROM Designed for UHF RFID Tag Chip"* ,ETRI Journal, Volume 30, Number 3,pp. 347-354, June 2008

Books

1. Frank Thornton, Brad Haines, Anand M. Das, Hersh Bhargava, Anita Campbell and John Kleinschmidt**,** ***"****RFID Security"*, Syngress Publishing, Inc., 2007
2. Cristian Puget, "*Low Power Processors & System on Chip*", CRC Press, Taylor & Francis group, 2006
3. Klaus Finkenzeller *"RFID Handbook-Fundamentals and Applications in Contactless Smart Cards and Identification"*, Second Edition, John Wiley & sons, 2003