A Novel Approach OF Low Power and Area Efficient Carry Select Adder

T. Haribabu, R. Jayalakshmi and S. MadhavaRao

ABSTRACT:

*C*arry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only as light increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with logical effort and through custom design and layout in 0.18- m CMOS process technology. The results analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA.

Index Terms—Application-specific integrated circuit (ASIC), area-efficient, CSLA, low power.

I. INTRODUCTION:

Digital Adders are the core block of DSP processors. The final carry propagation adder (CPA) structure of many adders constitutes high carry propagation delay and this delay reduces the overall performance of the DSP processor. Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1].

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However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input 0 and 1, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with 1 in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the 2-bit Full Adder (FA) structure. The details of the BEC logic are discussed. This brief is structured as follows. The delay and area evaluation methodology of the basic adder blocks. SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area. This paper proposes a simple and efficient approach to reduce the maximum delay of carry propagation in the final stage. Based on this approach a 16, 32 and 64-bit adder architecture has been developed and compared with conventional fast adder architectures. This work identifies the performance of proposed designs in terms of delay-area-power through custom design and layout in 0.18um CMOS process technology [2], [9], [10],[11] Instead of using dual carry-ripple adders. a carry select adder scheme using an add-one circuit to replace one carry-ripple adder requires 29.2% fewer transistors with a speed penalty of 5.9% for bit length 17 =64. If speed is crucial for this 64bit adder, then two of the original carry-select adder blocks can be substituted by the proposed scheme with a 6.39'0 area saving and the same speed.[3]A carry-select adder can be implemented by using a single ripple carry adder and an add-one circuit instead of using dual ripple carry adders.

A multiplexer-based add-one circuit is proposed to reduce the area with negligible speed penalty. The proposed 64 bit carry-select adder requires 42% fewer transistors than the conventional arry-select adder [4],[12],[13].Carry-select method has deemed to be a good compromise between cost and performance in carry propagation adder design. However, conventional carry-select adder (CSL) is still area-consuming due to the dual ripple carry adder structure. The excessive area overhead makes CSL relatively unattractive but this has been circumvented by the use of add-one circuit introduced recently. In this paper, an area efficient square root CSL scheme based on a new first zero detection logic is proposed. The proposed CSL witnesses a notable power-delay and area-delay performance

improvement by virtue of proper exploitation of logic structure and circuit technique. For 64-bit addition, our proposed CSL requires 44% fewer transistors than the conventional one. Simulation results indicate that our proposed CSL can complete 64-bitaddition in 1.50 ns and dissipates only 0.35mW at 1.8V in TSMC 0.18μm CMOS technology[5].

II. DELAY AND AREA EVALUATION METHODOLOGY OF THE BASIC ADDER :

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

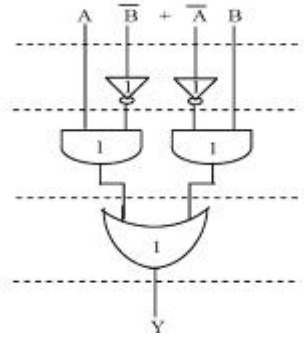


Figure I. Delay and area evaluation of an XOR gate

BEC

As stated above the main idea of this work is to use BEC instead of the RCA with cin 1 in order to reduce the area and power consumption of the regular CSLA. To replace the 3-bit RCA, an 4-bit BEC is required. A structure and the function table of a 4-b BEC are shownin Fig. 2 and Table II, respectively. Fig. 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as

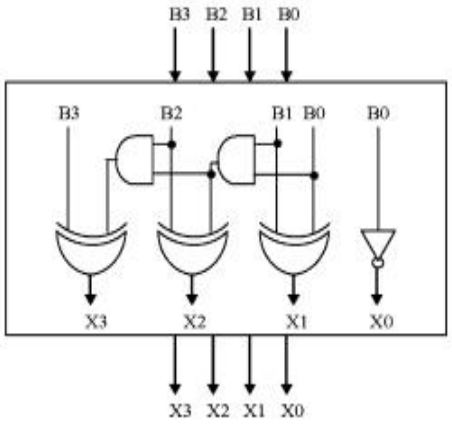


Fig. 2. 4-b BEC.

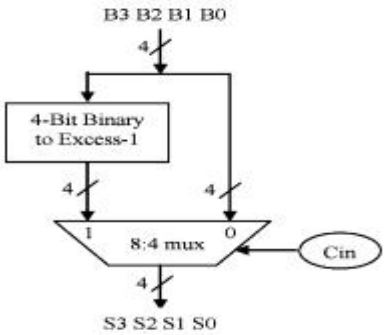


Fig. 3. 4-b BEC with 8:4 mux

TABLE I
DELAY ANDAREACOUNT OF THEBASICBLOCKS OFCSLA

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

TABLE II FUNCTIONTABLE OF THE4-b BEC

B[3:0]	X[3:0]
0000,0001…….1110,11111	0001,0010,……1111,0000

$$X0 = \sim B0$$
$$X1 = B0 \hat{} B1$$
$$X2 = B2 \hat{} (B0 \,\&\, B1)$$
$$X3 = B3 \hat{} (B0 \,\&\, B1 \,\&\, B2).$$

III. DELAY AND AREA EVALUATION METHODOLOGY OF REGULAR 16-B SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Fig. 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 5, in which the numerals within specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows. The group2] has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection i

TABLE III DELAY AND AREA COUNT OFREGULARSQRTCSLA GROUPS

Group	Delay	Area
Group2	11	57
Group3	13	87
Group4	16	117
Group5	19	147

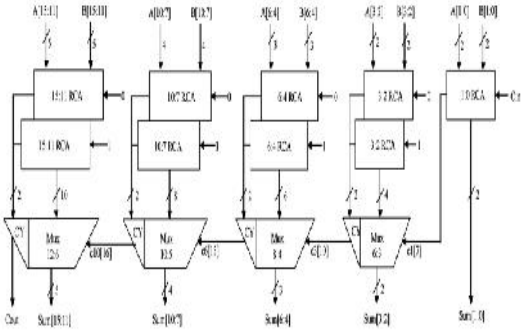
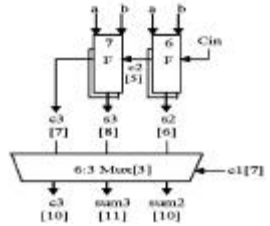
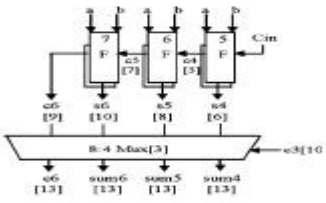


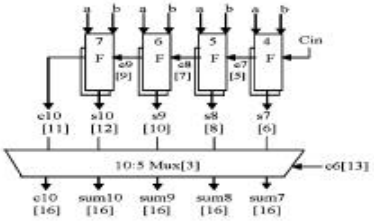
Fig. 4. Regular 16-b SQRT CSLA.



(a)



(b)



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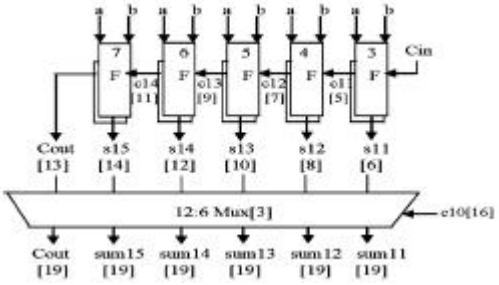


(d)

Fig. 5. Delay and area evaluation of regular SQRT CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. F is a Full Adder

1)The group2 has two sets of 2-b RCA based on the consideration of delay values of table 1the arrival of selection inputc1[time (t)=7] of 6:3mux is earlier than S3[t=8]and later than s2[t=6].Thus sum3[t=11]is simulation of s3 and mux [t=3]and sum2[t=10]is simulation of c1 and mux.

2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows:

$$\{c6, \mathrm{sum}[6:4]\} = c3[t=10] + \mathrm{mux}$$
$$\{c10, \mathrm{sum}[10:7]\} = c6[t=13] + \mathrm{mux}$$
$$\{\mathrm{cout},\ \mathrm{sum}[15:11]\} = c10[t=16] + \mathrm{mux}.$$

3) The one set of 2-b RCA in group2 has 2 FA for modifed sqrt and the other set has 1 FA and 1 HA . Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

Gate count

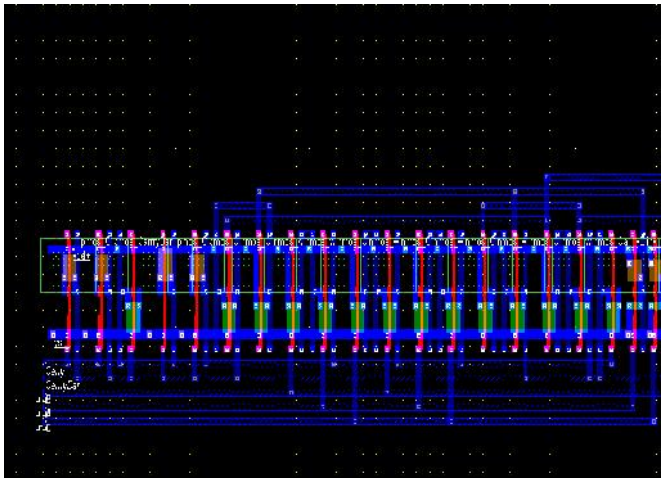
$$\text{Gate count} = 57\,(\mathrm{FA} + \mathrm{HA} + \mathrm{Mux})$$
$$\mathrm{FA} = 39(3 * 13)$$
$$\mathrm{HA} = 6(1 * 6)$$
$$\mathrm{Mux} = 12(3 * 4).$$

4) Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated.

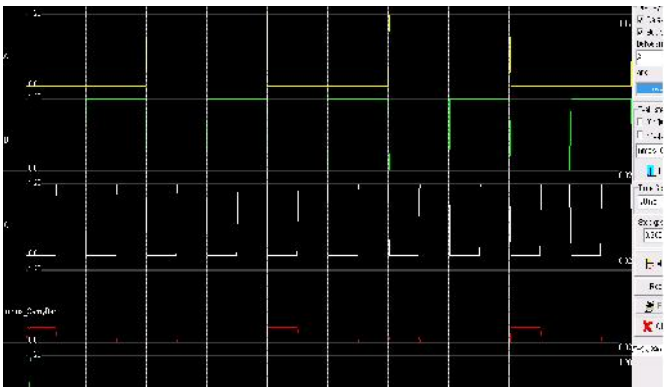
IV. Simulation Results:

The design proposed in this paper has been developed using Ver-ilog-HDL and synthesized in Cadence RTL compiler using typical li-braries of TSMC 0.18 um technology. The synthesized Verilog netlist and their respective design constraints file (SDC) are imported to micro wind SoC Encounter and are used to generate automated layout from standard cells and placement and routing [7]. Parasitic extraction is per-formed using Encounter's

NativeRCextraction tool and the extracted parasiticRC(SPEF format) is back annotated to Common Timing En-gine in Encounter platform for static timing analysis. For each word size of the adder, the same value changed dump (VCD) file is generated for all possible input conditions and imported the same to micro wind En-counter Power Analysis to perform the power simulations. The similar design flow is followed for both the regular and modified SQRT CSLA. Table V exhibits the simulation results of both the CSLA structures in terms of delay, area and power. The area indicates the total cell area of the design and the total power is sum of the leakage power, internal power and switching power. The percentage reduction in the cell area, total power, power-delay product and the area–delay product as func-tion of the bit size are shown in The total power consumed shows a similar trend of increasing reduction in power consumption 7.6%, 10.56%, 13.63%,and 15.46 % with the bit size. Interestingly, the delay overhead also exhibits a similarly decreasing trend with bit size. The delay overhead for the 8, 16, and 32-b is 14%, 9.8%, and 6.7% respectively, whereas for the 64-b it reduces to only 3.76%. The power–delay product of the proposed 8-b is higher than that of the regular SQRT CSLA by 5.2% and the area-delay product is lower by 2.9%. However, the power-delay product of the proposed 16-b SQRT CSLA reduces by 1.76% and for the 32-b and 64-b by as much as 8.18%, and 12.28% respectively. Sim-ilarly the area-delay product of the proposed design for 16-, 32-, and 64-b is also reduced by 6.7%, 11%, and 14.4% respectively.



LAYOUT FOR CARRY PFLA



OUTPUT WAVE FORM PFAL

V. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere tradeoff of delay for power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. It would be interesting to test the design of the modified 128-b SQRT CSLA. When we are using high bit rate calculations we going to adopt these architecture so that we can attain low power and high speed.

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