Optimization of Speed in Digital Circuits by Delay Error Detection using DETFFs with Parity Generator

R. Seetha, Mothkuri Sagar and Lanka Raja Ashwanth.

ABSTRACT

This paper gives an insight into the delay error detection circuit which ultimately increases the speed of the integrated circuit. This paper is based on conventional timing error methods which uses the warning window circuit. This paper also evaluates dynamic and transition error prevention. The delay data is monitored and error detected signal is generated. It is also useful to avoid the delay degradation due to the aging of the components. This paper evolution results indicates that the proposed flip flop has 10% or smaller area overhead low power consumption than the simple combination of the conventional DETFF (Dual Edge Triggered Flip Flop) and timing error detection method with parity generator circuit.

Keywords

VLSI-Very Large Scale Integration ,DETFF-Dual Edge Triggered Flip Flop,D-FF-D Flip Flop, CDN-Clock Distribution Networks
EDS-Error Detection Signal

I.INTRODUCTION

There is an increasing demand for very high speed (high clock frequency) circuits.These high speed circuits will consume more power at clock distribution networks which should be reduced. To increase the speed of the circuit and reduce the power consumption we need a DETFF.

DETFF is also called as Double Data Rate Flip Flop because they utilize both the rising and falling edges of the clock signal which increases the clock frequency (decreasing the time period to half) and reduces the power consumption at clock distribution networks to half. The power consumption rates of the recently proposed methods in VLSI are very efficient which reduced to half the previously existing rates. (previous rates-60%;currently 15~30%).

The following section gives a detailed notes of DETFFs. There are different types of DETFFs they are

i)DETFFs using duplicated flip flops
ii)DETFFs using pulsed clock generator
iii)DETFFs using C-elements.
Of the three the third type is preferred most due to its several advantages like power consumption and AC characteristics.

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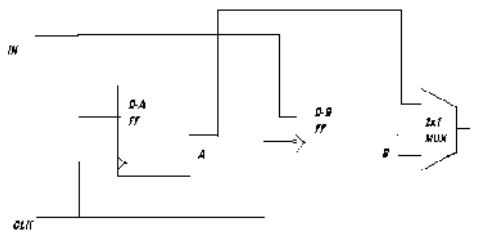
In any digital circuits, timing errors are given the utmost preference. These errors occur due to several reasons like voltage fluctuations, temperature variations and aging degradations. Any proposal put forward should be liable to different view points like the working of the circuit, errors occurring and the correction of errors of the digital circuit. This paper gives a detailed description of each type of DETFF and also about the proposed method of parity generator which lead to the optimization of area, speed and other key factors and also the method of detecting timing errors with parity generator.

II.BACKGROUND

This section gives the description of the various types of DETFFs and a brief note of parity generator.

DETFF:
i) DETFF using duplicated filp flops:

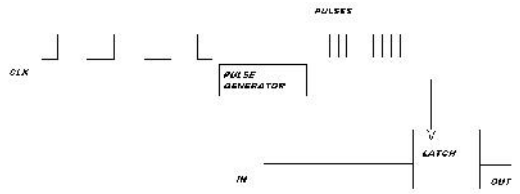
This type of DETFF uses two single two single edge triggered flip flops. One is active during the rising edge of the clock and the other is active on the falling edge of the clock signal. At each rising and falling edge of the clock the input values are assigned to the flip flops, then it is followed to the output of the circuit through a 2x1 MUX and this value will be the same till the next clock cycle. The disadvantage of this circuit is it will occupy more space and requires more power.



DETFF using duplicated FFs

ii) DETFF using pulsed clock generator:

Pulsed clock DETFFs can be classified into Explicit pulsed DETFFs and Implicit pulsed DETFFs. The Explicit pulsed DETFF is shown in the diagram below.

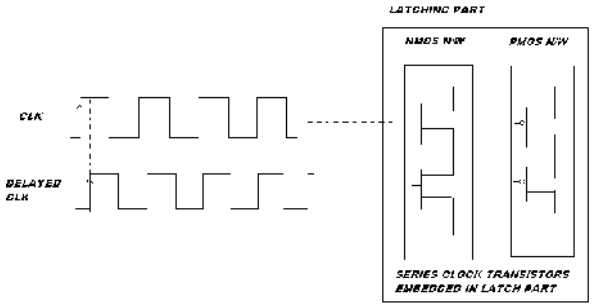


DETFF using explicit pulsed clock

Q1	Q2	Output
0	0	0
0	1	Previous value
1	0	Previous value
1	1	1

In this method also the frequency is halved but the clock distribution network increases as the each clock edge is replaced two edge pulses. This will increase the load on the clock as well as it increases the activity factor of the clock pulses. The disadvantage of this method is it increases the power consumption in CDNs.

Implicit pulsed DETFFs use two series devices embedded in the logic branch receiving a clock and a delayed respectively as shown in the diagram below.



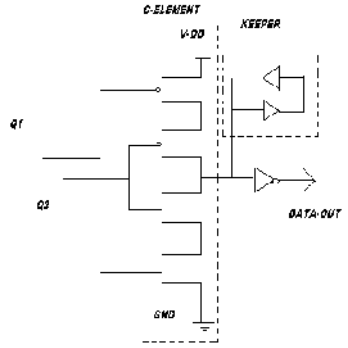
DETFF using implicit pulsed clock

In this method also the load is increased due to the additional transistor and delayed clock signal is increased in the clock distribution network which will increase the power consumption in the circuit.

iii)DETFFs using C-element:

C-element:

C-element is an asynchronous logic component originally designed by DAVID E. MULLER . It applies logical operations on the inputs and has hysterisis (predicts the output based on the history of the internal states). The output of the C-element reflects the inputs when all the inputs match. The output remains in that state until all the inputs make a transition. It consists of a pull-up and pull-down transistor combinations connected together. The diagram and working of the C-element is given below.

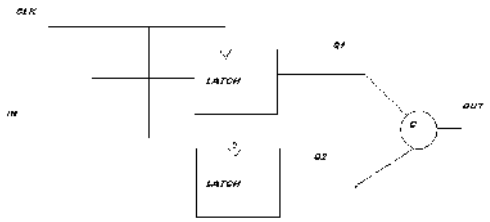


C-element structure

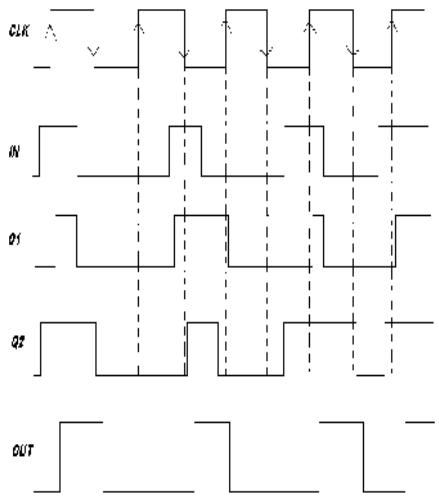
Truth table of C-element.

The C-element can be associated with a weak keeper structure for having a feature of storage in the C-elements.

DETFF using C-element is advantageous when compared to the other two types in terms of reducing area and power consumption. The area of the digital circuit is reduced to half of the DETFF using duplicated flip flops. The diagram and the timing chart of DETFF using C-element is given below.



DETFF using C-element



TIMING diagram

The working of the circuit is as described. On the rising edge of clock, low level sensitive latch becomes a closed switch and thus the output if flip flop is equal to that of this closed latch. This closed low level becomes transparent on the falling edge. At the same time, both the latches come to be the same as the value of IN and also the output.

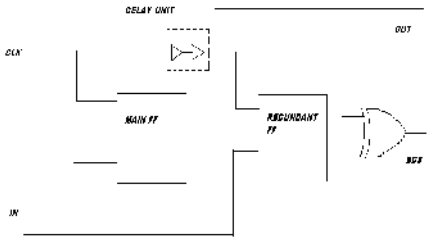
III.PREVIOUS METHODS OF TIMING ERROR DETECTION (Delay Error Detection):

The digital circuit becomes very easy to analyze when there is no consideration of errors (like timing errors). But in general there results certain errors due to various reasons like supply voltage variations temperature variations and aging degradations (NBTI-Negative Bias Temperature Instability).

When a circuit is absolute error free, then the transition of input signal of every flip flop occur before the corresponding changes of the clock signal. But when the circuit is analyzed including errors, it is observed that the transition of the input signal occur after the change of the clock signal. Such errors are detected by the parity generator circuit.

The parity generator employs an XOR gate along with a transition detector/window generator. The parity generator circuit uses "specified time (time factor)" as a parameter. If the transition of the input signal takes place after this specified time, an error is detected by the circuit. The error detection is done by the following two different methods as described below.

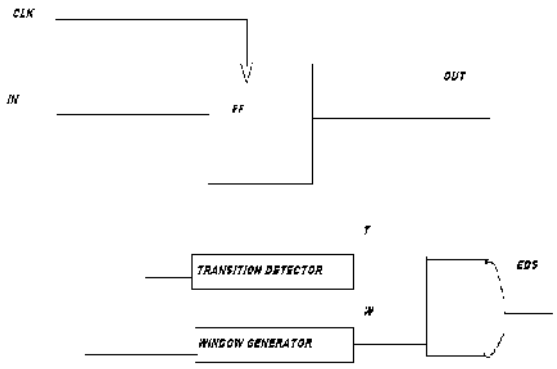
The first method of detection is by using Redundant flip flops. The diagram and the working of the detecting unit employing redundant flip flops is shown below.



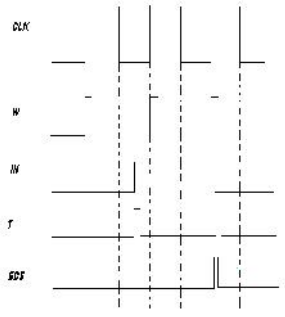
ERROR DETECTION using Redundant flip flop

As shown in the diagram above the clock input is delayed. The redundant flip flop receives the input value after a specified time due to the delay in the clock signal. If the flip flops (main and redundant) capture the input values before or after the specified time parameter, the error is given by the error detection signal EDS

The second method employs window generator circuit (windowing technique). The diagram and the working of the circuit are explained below.



ERROR DETECTION using WINDOW generator



TIMING diagram

In this method it employs window generator circuit. Here the transition detector follows the input value and that of the

window generator follows clock signal. From the circuit it is evident that if both value to a logic1 at the same time, EDS results in a logic1 (as shown in the timing diagram), otherwise no error is detected. The two blocks namely window generator and transition detector are explained below.

TRANSISTOR DETECTOR/WINDOW GENERATOR

The transistor detector is a circuit that generates or converts clock signals' rising edge to a very narrow pulse. It consists of a delay gate (delays clock signals) and then the clock signal is passed through a NAND gate and then inverted. In this the width of resulting pulse is equal to the width of delay time (specified time parameter).

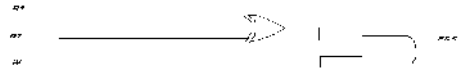
While the window generator resembles the transistor detector in design, the feature that makes this different from the latter (transistor detector) is the width of the resulting pulse is adjusted at the users desire. The design of the window generator is shown below.

Transition detector/Window generator

The general method of employing delay in digital systems is the use of logic gates (buffer or inverter or any logic gate). In order to provide larger delay time, large number of gates are required which lead to area overhead. Hence it is better to avoid using delay elements to the most extent.

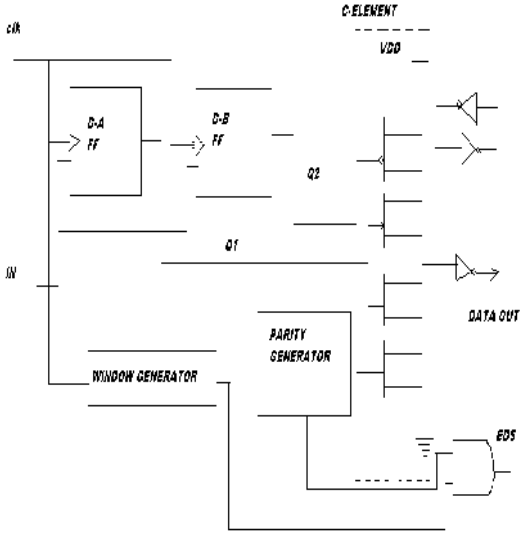
IV.PROPOSED DELAY EROR DETECTION USING DETFF AND PARITY GENERATOR

The proposed method employs the most efficient techniques available in VLSI technology. From the above listed three methods the third method of DETFF that uses C-elements found to be the most efficient in terms of power saving, increasing speed and reducing the area overhead. For the timing error detection, the parity generator circuit using window technique is employed. In the proposed method, the error detection unit is supplied with the outputs of two latches and a clock signal is passed through a windowing circuit. The different feature in the proposed method from previous methods is the design of error detection unit. The error detection unit in this proposed method is designed using parity generator that consists of an XOR gate and an AND gate as shown in the diagram below. The first diagram here shows the error detection unit and later the proposed method design along with its timing is given..

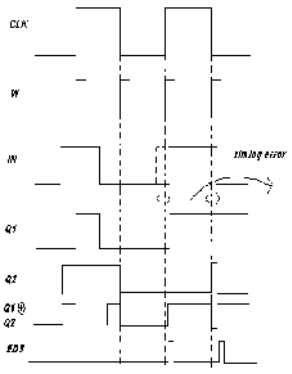


ERROR DETECTION UNIT

As shown in the diagram above the outputs of the latches are given to the XOR gate whose output is further connected as an input to the AND gate. The second input to the AND gate comes from the window generator. The output of the AND gate comes high when both the signals (inputs) come to high at the same time as shown in the timing diagram.



PROPOSED DETFF WITH ERROR DETECTION UNIT(Parity generator)



TIMING diagram of Proposed method FF

V.EVALUATION

There can exist various methods of detecting the timing errors. By using the various combinations one can have a design to detect the timing errors, but its always said to go for the most efficient in the VLSI technology. So, one can use different combinations from the existing types of DETFFs and also from the types of detecting errors. The circuit is designed
on a 45nm predictive technology model and simulated by HSPICE. During the evaluation the following parameters are specified to their predefined values as given VDD supply=1.1V, room temperature at 27^ C and clock frequency=1.25 GHz. The delay time of all delay elements is set as 0.1ns.
The following table gives the details of various parameters (area, power, set-up time, hold time and Clk-Q delay)

Methods	Area	Power consumption	Set-up time	Hold time	Clk-Q delay
C-element+ window generator	1	1	1	1	1
C-element+ redundant FFs	0.93	0.88	1.00	1.00	1.24
Proposed combination method	0.80	0.83	1.02	1.02	1.24

VI.CONCLUSION

This paper has described the various methods of construction of dual edge triggered flip flops with a parity generator used to detect timing errors. the proposed method is based on the use of DETFFs using C-elements and warning window technique with a parity generator to detect timing errors. The proposed method reduces the power consumption and area overhead to nearly ten percent than those of the conventional methods.

VII.REFERENCES

[1] S. V. Devarapalli, P. Zarkesh-Ha, and S. C. Suddarth, "A robust and low power dual data rate (DDR) flip-flop using C-elements,"Proc. IEEE Int'l Symp. Qual. Electron. Des., pp. 147–150, Mar. 2010.

[2] P. Zhao, J. McNeely, P. Golconda, M. A. Bayoumi, R. A. Barcenas, and W. Kuang, "Low-power clock branch sharing double-edge triggered flip-flop,"IEEE Trans. Very Large Scale Integr. Syst., vol. 15, no. 3, pp. 338–345, Mar. 2007.

[3] S. K. Mohideen and J. R. Perinbam, "Design of low power double edge triggered D FF,"Proc. IEEE Int'l Conf. India Council, pp. 450–452, Dec. 2005.

[4] W. Chung, T. Lo, and M. Sachdev, "A comparative analysis of low-power low-voltage dual-edge-triggered flip-flops,"IEEE Trans. Very Large Scale Integr. Syst., vol. 10, no. 6, pp. 913–918, Dec. 2002.

[5] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and en-ergy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microproces-sors," Proc. IEEE Int'l Symp. Low Power Electron. Des., pp. 147–152, 2001.

[6] H. K. Alidash, S. M. Sayedi, and H. Saidi, "Low-power state-retention dual edge-triggered pulsed latch,"Proc. IEEE Iranian Conf. Electr. Eng., pp. 417–420, May 2010.

[7] D. Ernst, N. S. Kim, S. Das, S. Pant, R. Rao, T. Pham, C. Ziesler, D. Blaauw, T. Austin, K. Flautner, and T. Mudge, "Razor: a low-power pipeline based on circuit-level timing speculation,"Proc. IEEE/ACM Int'l Symp. Microarchitecture, pp. 7–18, Dec. 2003.

[8] T. Sato and Y. Kunitake, "A simple flip-flop circuit for typical-case designs for DFM,"Proc. IEEE Int'l Symp. Qual. Electron. Des., pp. 539–544, Mar. 2007.

[9] M. Agarwal, B. C. Paul, M. Zhang, and S. Mitra, "Cir-cuit failure prediction and its application to transistor aging,"Proc. IEEE VLSI Test Symp., pp. 277–286, May 2007.

[10] B. P. Das and H. Onodera, "Warning prediction sequen-tial for transient error prevention," Proc. IEEE Int'l Symp. Defect & Fault Tolerance VLSI Syst., pp. 382– 390, Oct. 2010.

[11] S. E. Esmaeili, A. J. Al-Khalili, and G. E. R. Cowan, "Dual-edge triggered energy recovery DCCER flip-flop for low energy applications," Proc. IEEE Eur. Conf. Circuit Theory Des., pp. 57–60, Aug. 2009.

[12] [Online]. Available: http://www.eas.asu.edu/

[13] A. Balijepalli, S. Sinha, and Y. Cao, "Compact mod-eling of carbon nanotube transistor for early stage process-design exploration," Proc. Int'l Symp. Low Power Electronics & Des., pp. 2–7, 2007.

[14] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45nm early design explo-ration,"IEEE Trans. Electron Devices, vol. 53, no. 11, pp. 2816–2823, Nov. 2006.

[15] Y. Cao, T. Sato, D. Sylvester, M. Orshansky, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit simulation," Proc. IEEE Custom Integr. Circuit Conf., pp. 201–204, 2000.

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