Hspice Implementation of CNTFET Digital Gates

Sameer Prabhu and Nisha Sarwade

ABSTRACT : Carbon Nanotube (CNT) is one of the emerging technologies within nano technology, that is showing high efficiency and very wide range of applications in many different streams of science and technology. The Carbon Nano Tube Field Effect Transistors (CNTFETs) have been explored and proposed to be the promising candidate for the next generation of integrated circuit (IC) devices. Carbon Nano Tube Field Effect Transistors (CNTFETs) are being widely studied as possible successors to silicon MOSFETs. This paper focuses on modelling of CNTFET and using this model various digital circuits are simulated. This standard model has been designed for unipolar, MOSFET-like CNTFET devices. Hspice simulations have been performed on the logic gates designed using the modelled CNTFET.

Keywords - Carbon Nanotube, Carbon Nanotube Field Effect Transistor, modelling, Logic gates.

I. INTRODUCTION

As CMOS continues to scale deeper into the nanoscale, various device non idealities cause the I-V characteristics to be substantially different from well-tempered MOSFETs. For example, the source/drain series resistance is now a significant component of the total on-resistance. Proposals of metal contacted (Schottky) source/drain UTB SOI FET also alter the I-V characteristics significantly. Novel non-Si devices such as the carbon nanotube FETs (CNFETs) operate with completely different device physics with quasi-ballistic transport in the channel and Schottky barriers at the source/drain contacts[1]. CNTFETs are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the former devices is formed by CNTs instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon. In this paper, section II Introduces the Carbon nanotubes, section III delves into the CNTFET and modelling aspects of CNTFET. Simulation results of NOT, NAND and NOR are in section IV. Finally, Sections V discuss the conclusion and future scope.

Sameer Prabhu and Nisha Sarwade are with Department of Electrical Engineering, VJTI Mumbai, Email: sameerprabhu13@gmail.com, nishasarvade@vjti.org.in)

II. CARBON NANOTUBE (CNT)

Carbon is a Group 14 element that resides above silicon in the Periodic Table. Like silicon and germanium, carbon has four electrons in its valence shell. When carbon atoms are arranged in crystalline structures composed of hexagonal benzene-like rings, they from a number of allotropes that offer exceptional electrical properties. In their semiconducting forms, these carbon nonmaterial's exhibit room-temperature mobilities over ten times greater than silicon. In addition, they can be scaled to smaller feature sizes than silicon while maintaining their electrical properties.

Carbon nanotubes were discovered by S. Ijiima in 1991 [2] while performing some experiments on molecular structure composed of carbonium. CNTs are hollow cylinders composed of one or more concentric layers of carbon atoms in a honey comb lattice arrangement. It can be classified into SWCNT (Single Walled Carbon Nano Tube) and MWCNT (Multi Walled Carbon Nano Tube) shown in Figure 1.

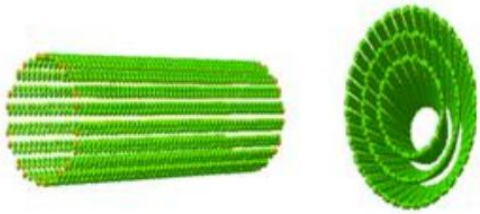


Fig.1: SWCNT and MWCNT

The way that graphene is rolled is described by a pair of indices (n, m), which are called "chiral vector". According to the chiral vector of a CNT, it can be determined whether it's a metallic or semiconducting CNT as shown in Figure 2.

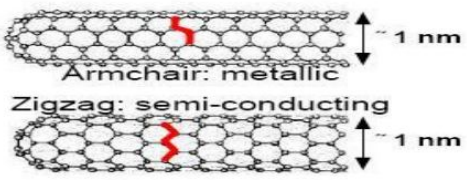


Fig.2: metallic and semiconducting CNT

III. Carbon Nanotube Field Effect Transistor (CNTFET)

A silicon wafer is covered with a thick silicon-dioxide film and then fabricated gold or platinum electrodes on it using standard semiconductor manufacturing technique. A single carbon nanotube was then positioned as a channel between two electrodes which are source and drain[3]. The underlying silicon wafer, heavily doped with impurities to make it good conductor, served as gate electrode. Applying the appropriate voltage to gate the nanotube is on or off. The first carbon nanotube field-effect transistors (CNTFETs) were reported in 1998, figure 3 shows the structure of CNTFET. There are several types of CNTFETs, but CNTFET geometries may be grouped in two major categories: planar and coaxial CNTFET.

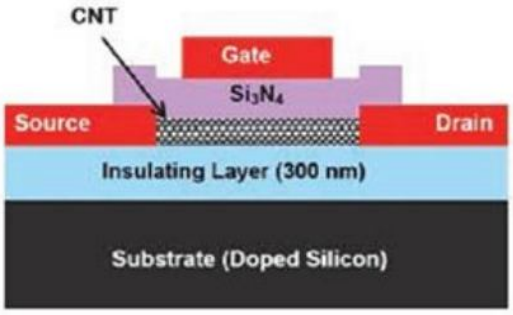


Fig.3:structure of CNTFET

In terms of the device operation mechanism, CNFET can be categorized as either Schottky Barrier (SB) controlled FET (SB-CNFET) or MOSFET-like FET[4]. The conductivity of SB-CNFET is governed by the majority carriers tunnelling through the SBs at the end contacts. The on-current and thereby device performance of SB-CNFET is determined by the contact resistance due to the presence of tunnelling barriers at both or one of the source and drain contacts, instead of the channel conductance. SB-CNFET shows ambipolar transport behaviour. On the other hand, MOSFET-like CNFET exhibits unipolar behaviour by suppressing either electron (pFET) or hole (nFET) transport with heavily doped source/drain.

A model is developed for nanoscale devices and circuits[5], including both CMOS technology beyond the 45 nm node and carbon nanotube field effect transistors (CNFETs), with the aim of guiding nanoscale device and circuit design. This model, provides large device speed improvement (6×for nFET and 14×for pFET) of CNFET over CMOS technology at the device level is significantly degraded(by a factor of 5 to8) by interconnect capacitance in a real circuit environment. The quasi-1D structure provides better electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device(e.g. fully depleted SOI). A MOSFET-like CNFET device structure shown in Figure 4 is used for the modelling because of both the fabrication feasibility and superior device performance of the MOSFET-like CNFET as compared to the SB-controlled FET.

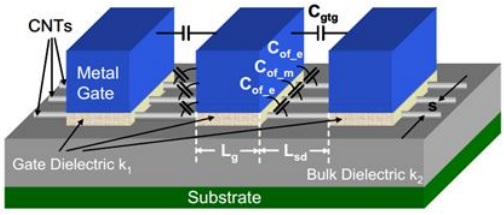


Fig.4: *The 3-D structure of MOSFET like CNFETs with multiple channels*

The complete CNFET device model[6] is implemented hierarchically in three levels. Device non-idealities are included hierarchically at each level. Level 1, models the intrinsic behaviour of MOSFET-like CNFET. The second level, denoted as includes the device non-idealities: the capacitance and resistance of the doped S/D CNT region, as well as the possible Schottky Barrier(SB) resistances of S/D contacts. The first two levels deal with only one CNT under the gate. The top level, i.e. level 3 models the interface between CNFET device and CNFET circuits. This level deals with multiple CNTs per device, and includes the parasitic gate capacitance and screening due to adjacent CNTs.

IV. SIMULATION RESULTS

This model is designed for unipolar MOSFET like CNTFET devices, where each device may have one or more carbon nanotubes. 32nm technology with (19,0) semiconducting with 1.5nm diameter CNT is used . The supply given is 0.9V and gate and drain voltage can be varied upto supply voltage. Figure 5,6 shows current voltage characteristics of CNT model. Gate voltage starting from zero is varied upto supply voltage with a variation of 0.01 x supply. Different curves for various value of Vdd with a variation of 0.1 x supply is shown.

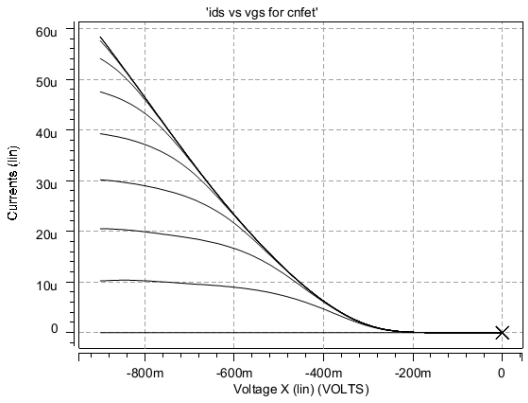


Fig 5: P channel CNT

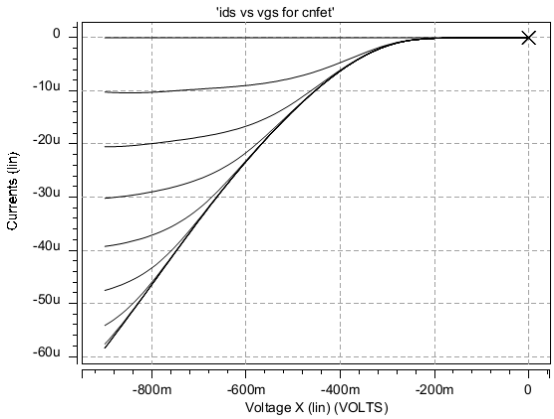


Fig 6: N channel CNT

Figure 7 shows an inverter comprising of P-type and N-type CNTFETs. They are coupled together in series between a high supply voltage V_{DD} and a low supply reference V_{SS}, as shown.

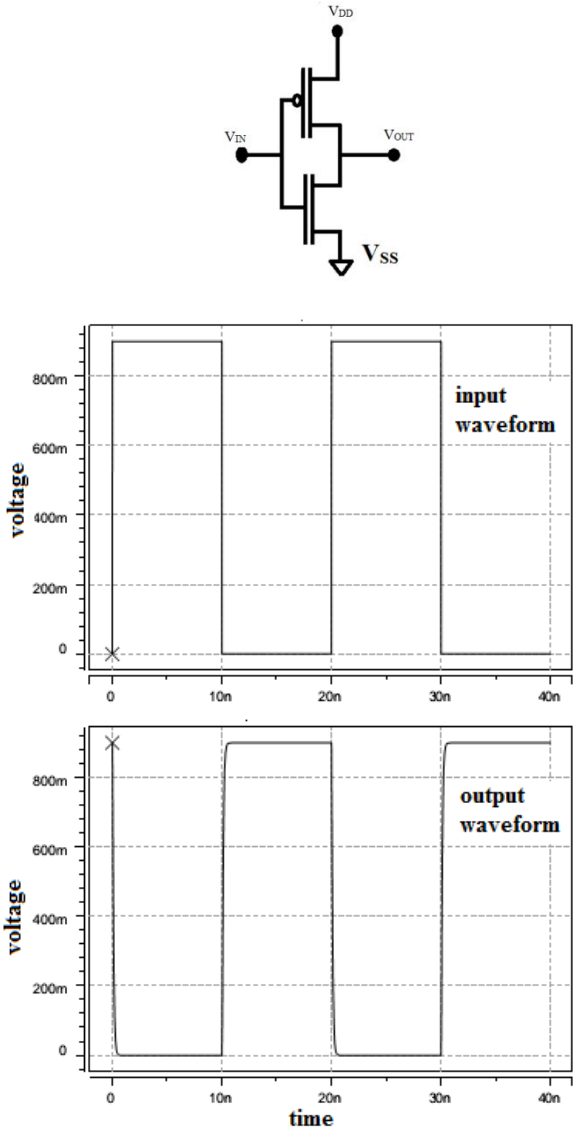


Fig 7: Structure of CNTFET NOT Gate and its behaviour

Figure 8 shows NAND gate comprising of CNTFETs. It comprises of driver CNTFETs coupled together in parallel between a high supply reference V_{DD} and a series active load transistors, which is coupled to a low supply reference V_{SS} as shown.

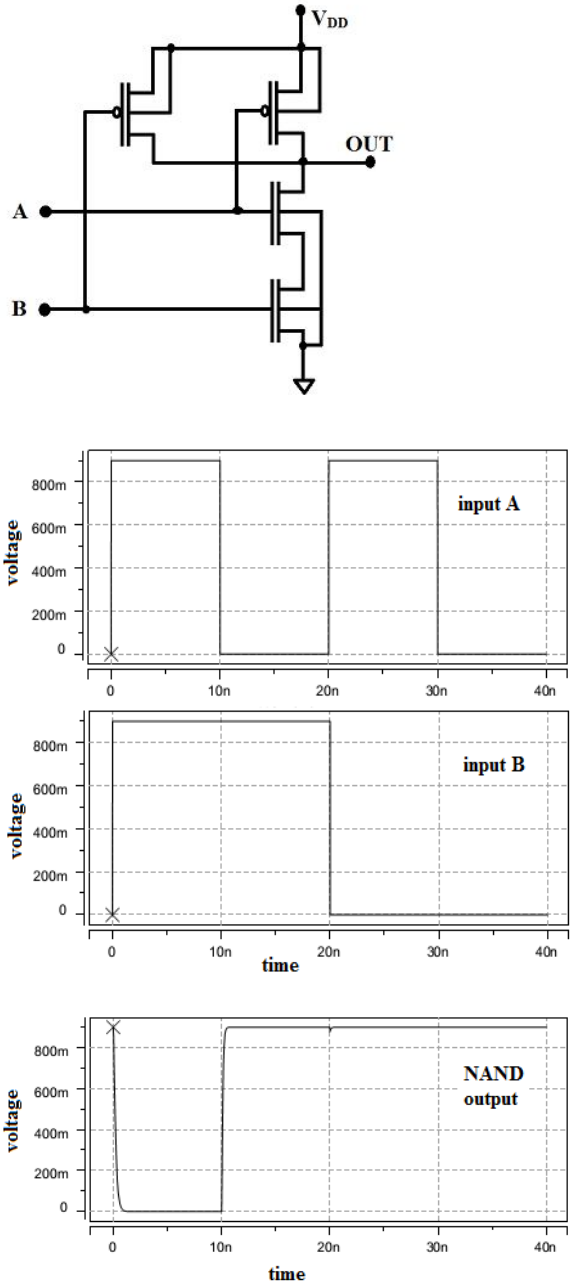
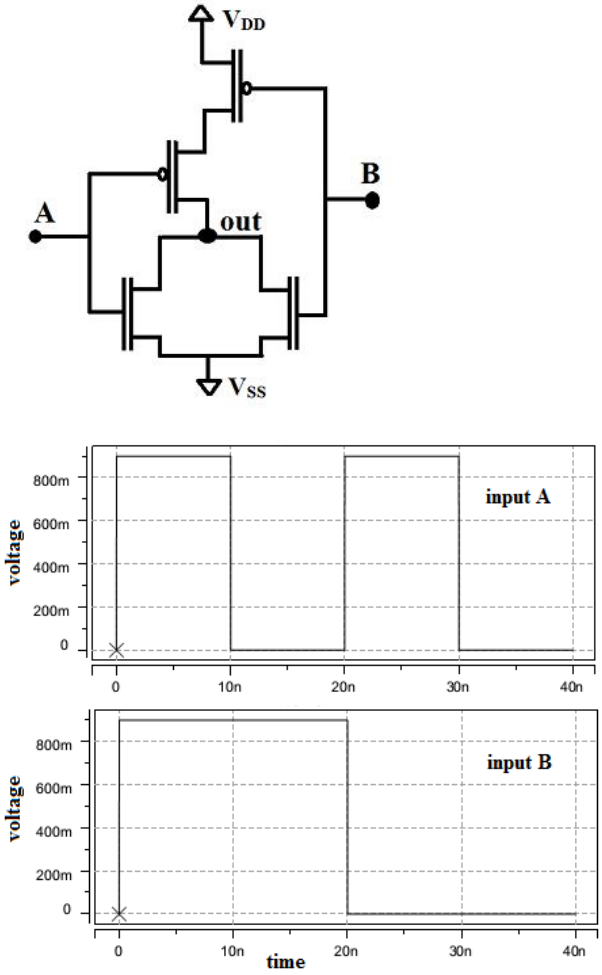


Fig 8: Structure of CNTFET NAND Gate and its behaviour

Figure 9 shows NOR gate comprising of CNTFETs. It comprises of driver CNTFETs coupled together in series between a high supply reference V_{DD} and a parallel connected active load transistors, which is coupled to a low supply reference V_{SS}, as shown.

V. CONCLUSION AND FUTURE SCOPE

This paper adequately explains the various modelling aspects of the proposed CNTFET. The various circuits such as NOT, NAND, NOR gates designed using CNTFET. Basic functions such as AND, OR in CMOS technology are implemented by generating related inverted functions (e.g., NAND, NOR) followed by an inverter. Voltage threshold losing which occurred in passing high and low voltages in NMOSFET and PMOSFET, respectively results in such implementation. CNFET technology provides more efficient way to implement these functions in terms of delay, power consumption and area. Voltage threshold is proportional to the $1/D_{CNT}$, so increasing the diagonal of nanotube (i.e., D_{CNT}) results in decreasing the voltage threshold toward zero. Consequently, PCNFET and NCNFET could be utilized in pull-down and pull- up network, respectively. AND/OR circuits in CMOS technology include six transistors, whereas the number of transistors in CNFET based circuits reduce to four.



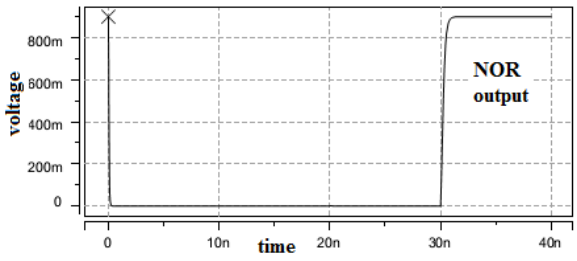


Fig 9: Structure of CNTFET NOR gate and its behaviour

REFERENCE

[1] C. Dwyer, M. Cheung, and D. J. Sorin, "Semi-empirical SPICE models for carbon nanotube FET logic," in Proc. Conf. Nanotechnology, Aug. 2004, pp. 386–388.

[2] S. Iijima, "Helical microtubules of graphitic carbon", Nature, vol.354, no.6348, Nov. 1991, pp.56-8.

[3] Ali Keshavarzi, Arijit Raychowdhury, Juanita Kurtin, Kaushik Roy, and Vivek De, "Carbon Nanotube Field-Effect Transistors for High-Performance Digital Circuits—Transient Analysis, Parasitic, and Scalability", IEEE Transactions On Electron Devices, Vol. 53, NO. 11, Nov-2006.

[4] J. Deng, H.-S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application - Part I: Model of the Intrinsic Channel Region," IEEE Trans. Electron Devices, vol. 54, pp. 3186-3194, 2007.

[5] Fabien Pregaldiny et.al.,—Compact Modelling and Applications of CNTFETs for Analog and Digital Circuit Design‖, IEEE Trans. Elec.dev., pp. 1030–1033, 2006.

[6] J. Deng, H.-S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application - Part II: Full Device Model and Circuit Performance Benchmarking," IEEE Trans. Electron Devices, vol. 54, pp. 3195-3205, 2007.