Computer-Aided Noise modeling, analysis and optimization of a SiGe HBT based Input Buffer

Santosh Kumar Patnaik

Abstract: This article presents the computer aided noise modeling, analysis and optimization of an Input Buffer designed using SiGe heterojunction bipolar transistor (HBT), intended to be used in a high speed Track and Hold Amplifier (THA). This is done by noise matrix manipulation using MATLAB programme. This helps in better understanding the noise involvement with the circuit. Direct parameter extraction technique is used to obtain all the extrinsic and intrinsic parameters of the SiGe HBT. Extracted parameters are then used in the MATLAB programme to obtain the input referred noise voltage of the Input Buffer. The programming involves in breaking the small-signal equivalent circuit of the Input Buffer including the noise sources into many smaller blocks. These smaller blocks may either contain a voltage control current source (VCCS), a resistor, or a capacitor. To get the final output, these blocks are combined either in parallel, or in series, or in cascade (chain) configuration depending on how these parameters are connected in the circuit. Here Z, Y, and ABCD-parameters are used to do the matrix operation. Also, parameter conversions are required when two blocks of different configurations are combined. The validity of the results obtained from the MATLAB programme is done after comparing them with the simulated results obtained through SPICE. Both the results are in good agreement with each other.

Keywords: SiGe, HBT, ADC, SNDR, THA, Input Buffer, SEF

I. INTRODUCTION

The study of noise in electronic circuit is important because it represents a lower limit to the size of the electrical signal that can be processed by a circuit without significant deterioration in signal quality. Noise also results in an upper limit to the useful gain of an amplifier. In an electronic circuit, resistors, transistors, conductors etc. are the prime cause of noise. There are many types of noise which are involved with the electronic components out of which shot noise and thermal noise are the predominant noises [1].

For any electronic circuit, noise calculation can be done using either nodal analysis or mesh analysis with the help of Kirchhoff's voltage law or current law respectively. This method is very simple as long as the circuit is small. With the increase in the number of nodes or meshes in the circuit, this method becomes complicated and a tedious process is required to get a mathematical noise model of the circuit [1]. Noise matrix is used to overcome this problem and to calculate the overall noise of the electronic circuit in terms of input referred noise voltage considering the noise associated with each component present inside the electronic circuit.

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A specific architecture along with Signal-to-Noise and Distortion Ratio (SNDR) plays an important role in determining the speed and resolution of an Analog-to-Digital Converter (ADC)[2]. High speed and moderate resolution ADCs are essential in the areas of data acquisition, satellite communication, radar processing, sampling oscilloscopes, high-density disk drives etc. For designing high speed ADCs, HBTs are preferred because of its high f_t and linearity [3] [4]. On the other hand, to improve the resolution, it is important to increase the SNDR of the ADC [2]. This improvement in SNDR can be started at the very first block of an ADC which is a THA. So, if the SNDR of a THA is improved, its resolution will also improve. This improvement in resolution of THA improves the resolution of the ADC.

A THA consists of three main blocks: an Input Buffer, a Switch and an Output Buffer [2] [5] [6] as shown in Fig. 1.

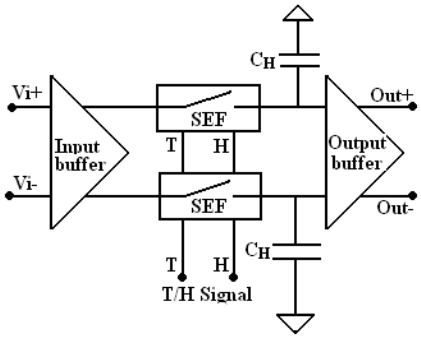

Figure 1: Block diagram of a THA

A Switch is used to do the sampling. It can be implemented using an emitter follower, popularly known as Switched Emitter Follower (SEF). Input Buffer is used to keep the SEF isolated from the input signal and Output Buffer acts as an intermediate block between THA and rest of the ADC. The Input Buffer used for our THA is a differential amplifier having unity gain. To improve the resolution of the THA, its SNDR must be kept as low as possible. Out of these three blocks the noise and distortion level of Input Buffer has to be minimized to allow the THA to have a good resolution as it is exposed directly to the input signal.

In this article, the noise behavior of an Input Buffer has been explored using computer-aided noise modeling. Noise analysis has been done to find out the input referred noise voltage of the Input Buffer designed with SiGe HBT with a view to use it in our designed THA which will operate at 3 GSample/s and the resolution should not be less than 10-bit. Intrinsic and extrinsic parameters of SiGe HBT required in the noise modeling are obtained through direct parameter extraction method from the measured S-parameters [7]-[20].

The extraction of parameters has been done in a frequency range of 1-50 GHz. Further, the input referred noise voltage level has been optimized using mathematical noise modeling.

This article has been arranged in the following manner. Section II presents the steps to obtain the input referred noise voltage of the Input Buffer. Section III describes the extraction of intrinsic and extrinsic parameters of SiGe HBT. In Section VI, computer-aided noise modeling is illustrated. Results and discussion are given in Section V. Finally Section VI concludes the article.

II. STEPS TO CALCULATE INPUT REFERRED NOISE VOLTAGE OF INPUT BUFFER

1. A schematic of THA circuit using SiGe HBT is implemented using SPICE [2] [5] [6].
2. Intrinsic and extrinsic parameters for SiGe HBT involved in the circuit are extracted using S-parameters [7]-[20].
3. Small-signal noise model by using noise voltages and currents for the differential Input Buffer is considered [1] [21]-[23].
4. Noise model is separated into discrete components and the electrical noise matrix is formed for each component [24]-[26].
5. Noise matrix of discrete components are combined as per the small-signal noise model given in step 4, using MATLAB programme [24]-[26].
6. Final output of MATLAB programme is multiplied with √2 to get the input referred noise voltage of the Input Buffer [1].
7. With this input referred noise voltage Fourier analysis is done to get the SNDR of the THA [2].
8. Optimization of the noise is done using mathematical noise modeling [27].
9. After optimization of the noise, steps 3 to 6 are repeated to obtain SNDR of the THA.
10. Resolution of the THA is calculated by comparing the results of steps 6 and 8 [2].

III. EXTRACTION OF INTRINSIC AND EXTRINSIC PARAMETERS OF SIGE HBT

For extracting the parameters of SiGe HBT direct parameter extraction method is preferred over numerical optimization because of its uniqueness and efficiency. For this purpose, hybrid-π equivalent model is used. The small-signal equivalent model of the SiGe HBT is shown in Fig. 2 [7]-[20].

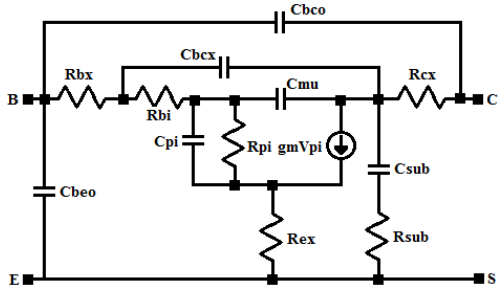

Figure 2: Small-signal equivalent circuit model for a SiGe HBT

To extract the extrinsic resistances, HBT must be operated in over driven I_B bias condition. Under this condition the equivalent small-signal circuit reduces to a resistive network. The extrinsic resistances can be described by the Z-parameter of the circuit employing following equations [12];

$$R_{bx} = real(Z_{11} - Z_{12}) \quad (1)$$

$$R_{ex} = real(Z_{12}) \quad (2)$$

$$R_{cx} = real(Z_{22} - Z_{21}) \quad (3)$$

The parasitic capacitance extraction is done under cold mode operation [12]. The equivalent circuit under this condition reduces to a capacitive network. The Y-parameters for this equivalent circuit are;

$$\omega\left(C_{pi} + C_{beo}\right) = \mathrm{Im}(Y_{11} + Y_{12}) \quad (4)$$

$$\omega\left(C_{mu} + C_{bcx} + C_{bco}\right) = \mathrm{Im}(-Y_{12}) \quad (5)$$

To extract the intrinsic resistors and capacitors, the SiGe HBT ($0.21\text{x}0.84\mu m^2$) should be connected in cutoff mode (V_{BE} = 0 V with forward collector voltage V_{CE} = 3 V). With this mode the small-signal equivalent model of the HBT looks as shown in Fig. 3.

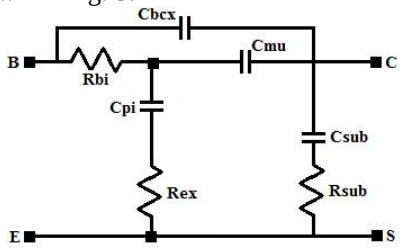

Figure 3: Small-signal equivalent circuit model for SiGe HBT biased in the cut off mode

The Y-parameters, obtained from the reduced equivalent circuit shown in Fig. 3, are given below [13];

$$Y_{11} = j\omega C_{bcx} + \frac{j\omega(C_{mu} + C_{pi})}{1 + j\omega R_{bi}(C_{mu} + C_{pi})} \quad (6)$$

$$Y_{12} = Y_{21} = -j\omega C_{bcx} - \frac{j\omega C_{mu}}{1 + j\omega R_{bi}(C_{mu} + C_{pi})} \quad (7)$$

$$Y_{22} = Y_{sub} + j\omega C_{bcx} + \frac{j\omega C_{mu}(1 + j\omega R_{bi} C_{pi})}{1 + j\omega R_{bi}(C_{mu} + C_{pi})} \quad (8)$$

From (6) and (7), R_{bi} and C_{pi} can be obtained as

$$R_{bi} = \mathrm{Re}\left[\frac{1}{Y_{11} + Y_{12}}\right] \frac{\mathrm{Re}(Y_{11} + Y_{12})}{\mathrm{Re}(Y_{11})} \quad (9)$$

$$\omega C_{pi} = -\mathrm{Im}\left(\frac{1}{Y_{11} + Y_{12}}\right)^{-1} \quad (10)$$

Fig. 4 shows the plot of extracted R_{bi} and C_{pi} with respect to frequency.

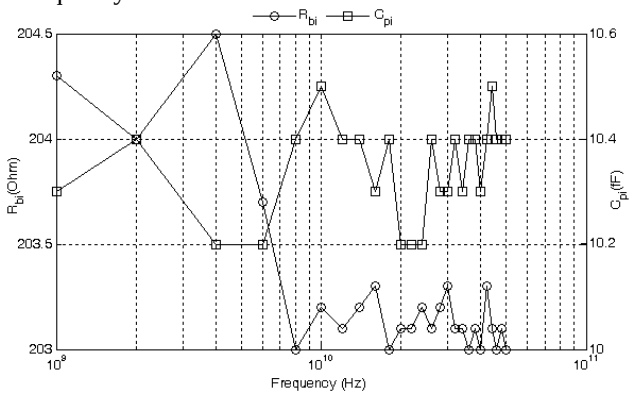

Figure 4: Plot of R_{bi} and C_{pi} vs. frequency

To extract the rest of the intrinsic parameters, HBT should operate in forward bias mode. Fig. 5 shows S-parameter data from the forward mode SiGe HBT in the frequency range of 1-50 GHz.

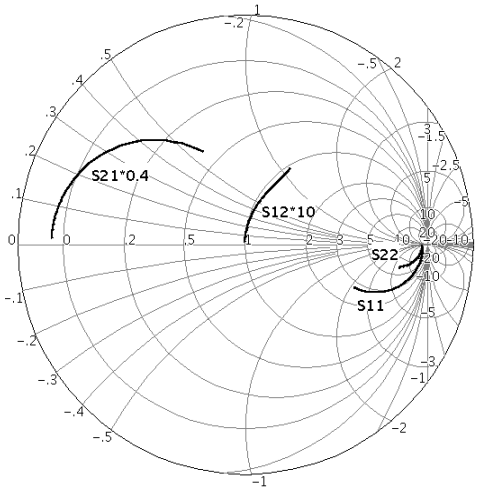

Figure 5: S-parameter data from the forward bias mode SiGe HBT in the frequency range of 1-50 GHz (V_{CE} = 3 V, I_C = 1.29 mA, V_{BE} = 450 mV)

The small-signal equivalent circuit of SiGe HBT under this forward bias mode is shown in Fig. 6 [13].

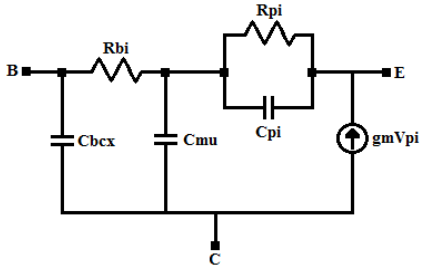

Figure 6: Small-signal equivalent circuit of SiGe HBT in forward bias mode

The ABCD-parameters for this equivalent circuit are;

$$A_{11} = 1 + R_{bi} Y_{bc} \quad (11)$$

$$A_{12} = \frac{1}{g_m + Y_{pi}}(1 + R_{bi} Y_{bc} + R_{bi} Y_{pi}) \quad (12)$$

$$A_{21} = Y_{bc} + Y_{ex} + R_{bi} Y_{bc} Y_{ex} \quad (13)$$

$$A_{22} = \frac{1}{g_m + Y_{pi}}\left(Y_{ex}\left(1 + R_{bi} Y_{bc} + R_{bi} Y_{pi}\right) + Y_{bc} + Y_{pi}\right) \quad (14)$$

where $g_m = g_{mo} \exp(-j\omega\tau)$, $Y_{pi} = \frac{1}{R_{pi}} + j\omega C_{pi}$,

$Y_{bc} = j\omega C_{mu}$, $Y_{ex} = j\omega C_{bcx}$

Utilizing (11)-(14), one can obtain;

$$\mathrm{Re}\left(\frac{A_{12}}{A_D}\right) = \sim R_{bi}\left(1 + \frac{C_{mu}}{C_{pi}}\right) \quad (15)$$

where $A_D = \left(A_{11} A_{22} - A_{12} A_{21}\right)$

Using the ABCD-parameters presented in (11)-(15), the intrinsic parameters of the SiGe HBT are calculated as given below;

$$\mathrm{Im}\left(A_{11}\right) = \omega R_{bi} C_{mu} \quad (16)$$

$$\mathrm{Im}\left(\frac{A_{11}}{A_{21}}\right) \sim \frac{-1}{\omega\left(C_{mu} + C_{bcx}\right)} \quad (17)$$

$$\frac{1}{R_{pi}} = \mathrm{Re}\left(\frac{A_{11}A_D}{A_{12} - A_D R_{bi}}\right) \tag{18}$$

$$g_m = \left(\frac{1 - A_D}{A_D}\right) Y_{pi} \tag{19}$$

$$g_{mo} = \sqrt{\mathrm{Re}(g_m)^2 + \mathrm{Im}(g_m)^2} \tag{20}$$

$$\tau = -\tan^{-1}\left(\frac{\mathrm{Im}(g_m)}{\mathrm{Re}(g_m)}\right) \times \frac{1}{\omega} \tag{21}$$

Fig. 7 shows the plot of R_{pi} and g_{mo} versus frequency.

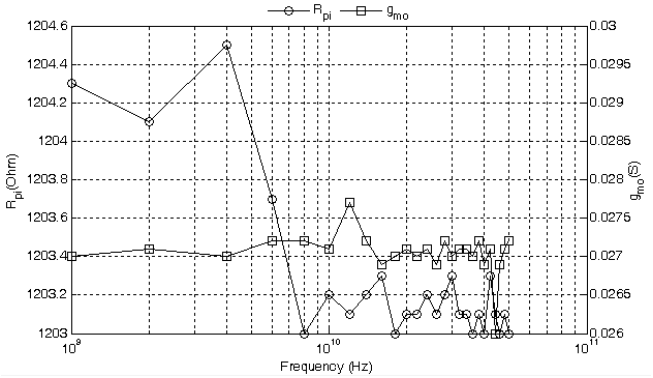

Figure 7: Plot of R_{pi} and g_{mo} vs. frequency

The extracted parameters with values are listed in Table 1.

Table 1: Extracted parameters of the SiGe HBT

Extracted Bias-Independent Parameters		Extracted Bias-Dependent Parameters (V_{CE} = 3V, I_C = 1.29mA, V_{BE} = 450mV)	
Parameter	Extracted Value	Parameter	Extracted Value
R_{bx}	54Ω	R_{bi}	203.2Ω
R_{cx}	6Ω	R_{pi}	1203.3Ω
R_{ex}	20Ω	C_{pi}	10.4fF
C_{beo}	0.34fF	C_{mu}	70fF
C_{bco}	0.62fF	C_{bcx}	97fF
		g_{mo}	28mS
		C_{sub}	29.31fF
		R_{sub}	2.31KΩ

IV. COMPUTER-AIDED NOISE MODELING

Fig. 8 shows the circuit schematic of the Input Buffer which is a differential amplifier with unity gain. Transistors Q1 and Q2 are the driver transistors and transistors Q3 and Q4 are used in diode configuration to overcome the V_{BE} modulation in the driver transistors Q1 and Q2, hence improves the linearity of the Input Buffer. In a differential amplifier, if both sides are considered symmetrical then the total input referred noise voltage of one side will be $\sqrt{2}$ times the input referred noise voltage of the differential amplifier [1].

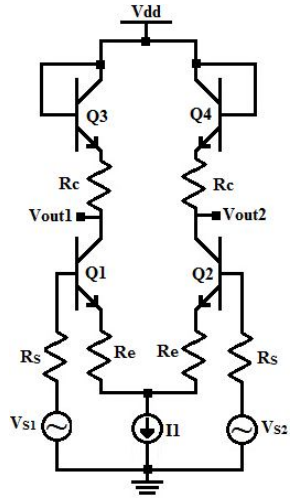

Figure 8: Circuit schematic of an Input Buffer

Using this concept, the electrical noise model for one side of the Input Buffer is drawn in Fig. 9 [1] [21]-[23].

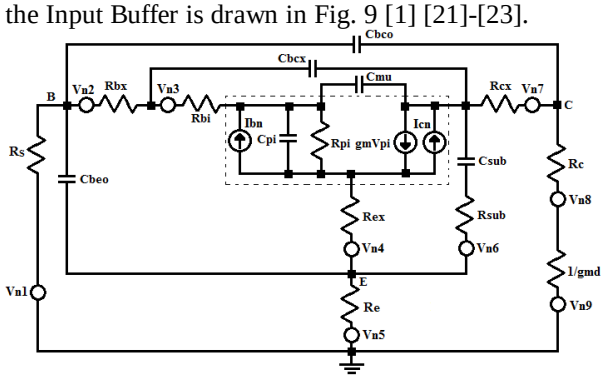

Figure 9: Electrical noise model representation of one side of Input Buffer

Voltages V_{n1}-V_{n9} are the thermal noise voltages associated with all the resistors. Currents I_{bn} and I_{cn} are the shot noise currents present in the HBT. The block present inside the dashed box shown in Fig. 9 is a VCCS.

Now, using noise correlation matrix, total input referred noise voltage of the electrical noise model, shown in Fig. 9, can be calculated. For obtaining the noise matrix, the electrical noise model is separated into several blocks containing VCCS, resistors and capacitors. In the noise matrix, the series, parallel and cascade combinations are written by using Z, Y and ABCD-parameter, respectively. All the combinations, conversion between parameters and matrix operations are done using MATLAB [24]-[26].

Tables 2(a)-(c) indicate the noise matrices used in MATLAB to determine the input referred noise voltage of the Input Buffer.

Table 2(a) Y-matrix for VCCS

VCCS_11 = (j.*omega.*Cpi)+(1/Rpi);	C_VCCS_11 = q*I_B.*ones(size(f));
VCCS_12 = zeros(size(f));	C_VCCS_12 = zeros(size(f));

VCCS_21 = g_{mo}.*ones(size(f));	C_VCCS_21 = zeros(size(f));
VCCS_22 = zeros(size(f));	C_VCCS_22 = q*I_C.*ones(size(f));

where "omega" is the angular frequency, "f" is the frequency of operation, "q" is the charge of an electron, "g_{mo}" is the transconductance of the circuit, "I_B" is the current flowing through the base of HBT, "I_C" is the current flowing through the collector of HBT. In Table 2(a), the content of the second column represents the noise correlation matrix associated with the matrix of the first column.

Table 2(b) Y-matrix for a Resistor

R_11 = (1/R).*ones(size(f));	C_R_11 = 2.*K.*T.*real(R_11);
R_12 = -(1/R).*ones(size(f));	C_R_12 = 2.*K.*T.*real(R_12);
R_21 = -(1/R).*ones(size(f));	C_R_21 = 2.*K.*T.*real(R_21);
R_22 = (1/R).*ones(size(f));	C_R_22 = 2.*K.*T.*real(R_22);

where "K" is the Boltzmann's constant and "T" is the temperature of operation.

Similarly for a Z-matrix of a resistor, R_11-R_22 will be "R" multiplied with "ones(size(f))" and the correlation matrix is the same as in Y-matrix.

Table 2(c) Y-matrix for a Capacitor

C_11 = j.*omega.*C;	C_C_11 = zeros(size(f));
C_12 = -j.*omega.*C;	C_C_12 = zeros(size(f));
C_21 = -j.*omega.*C;	C_C_21 = zeros(size(f));
C_22 = j.*omega.*C;	C_C_22 = zeros(size(f));

In case of a Z-matrix for a capacitor, C_11-C_22 will be "1/j.*omega.*C" and the correlation matrix is the same as in Y-matrix. Contents of the second column of Tables 2(b) and 2(c) represent the noise correlation component associated with the content of the first column. Using the matrices given in Table 2, a MATLAB programme has been written to find out the input referred noise voltage of half circuit of the Input Buffer. Multiplying the final output of MATLAB programme with a factor of $\sqrt{2}$, the total input referred noise voltage of the Input Buffer can be obtained. The MATLAB programme flow is given below;

1. Xa = VCCS [Y] + C_{mu} [Y] - Parallel Combination [No conversion]

2. Xb = Xa [Y] + R_{ex} [Z] - Series Combination [Xa is converted from Y to Z]

3. Xc = Xb [Z] + R_{bi} [Y] - Chain Combination [Xb is converted from Z to A and R_{bi} is converted from Y to A]

4. Xd = Xc [A] + Xy [Z] - Chain Combination [Xy is converted from Z to A]

   4.1. Xy = C_{sub} [Z] + R_{sub} [Z] - Series Combination [No conversion]

5. Xe = Xd [A] + C_{bcx} [Y] - Parallel Combination [Xd is converted from A to Y]

6. Xf = R_{bx} [Y] + Xe [Y] - Chain Combination [R_{bx} and Xe both are converted from Y to A]

7. Xg = Xf [A] + R_{cx} [Y] - Chain Combination [R_{cx} is converted from Y to A]

8. Xh = Xg [A] + C_{bco} [Y] – Parallel Combination [Xg is converted from A to Y]

9. Xi = C_{beo} [Z] + Xh [Y] – Chain Combination [C_{beo} is converted from Z to A]

10. Xj = Xi [A] + R_e [Z] – Series Combination [Xi is converted from A to Z]

11. Xk = R_S [Y] + Xj [Z] – Chain Combination [R_S is converted from Y to A and Xj is converted from Z to A]

    11.1. Xz = R_c [Z] + 1/g_{md} [Z] – Series Combination [No conversion]

12. Xout = Xk [A] + Xz [Z] – Chain Combination [Xz is converted from Z to A]

13. Xirn = $\sqrt{2}$ * Xout.

[Y – Admittance Parameter, Z – Impedance Parameter, A – ABCD parameter]

Xout is the input referred noise voltage of one side of the Input Buffer and Xirn is the input referred noise voltage of the complete Input Buffer.

V. RESULTS AND DISCUSSION

Fig. 10 shows the simulated input referred noise voltage of the Input Buffer.

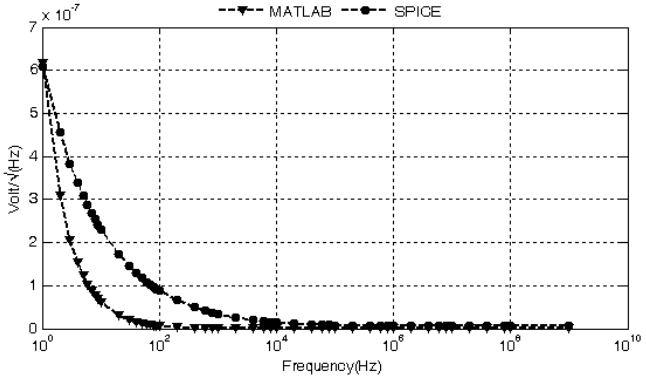

Figure 10: Input referred noise voltage of the Input Buffer

From Fig. 10 it is evident that both SPICE simulated and MATLAB simulated results are nearly equal and it is

approximately 621 nV/sqrt(Hz) at low frequency and decreases with the increase in frequency. With this value of input referred noise voltage the total SNDR of THA is 58.23 dB at 3 GHz sampling frequency. Therefore, the effective number of bits (ENOB) is 9.38 (resolution is 9-bit). This is 1 bit less than the desired 10-bit resolution.

To improve the resolution of the THA, the input referred noise voltage of the Input Buffer has to be reduced. This is done with the help of Noise Figure (NF). The overall NF of one side of the Input Buffer can be calculated by considering it as a series feedback amplifier as shown in Fig. 11 [27].

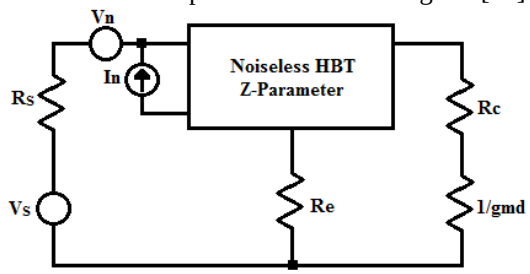

Figure 11: Series feedback amplifier with noise source

Considering the HBT as s noiseless block represented by Z-parameters, (22) and (23) represent the input referred noise voltage and current of HBT respectively and (24) is the noise voltage of source resistance R_S.

$$V_n = \sqrt{4KTA\Delta f} \tag{22}$$

$$I_n = \sqrt{4KTB\Delta f} \tag{23}$$

$$V_s = \sqrt{4KTR_S\Delta f} \tag{24}$$

The NF of the one side of the Input Buffer is;

$$NF = 1 + \frac{A}{R_S} + \frac{B}{R_S}\left|\frac{R_S Z_{21} + R_e(Z_{21} - Z_{11})}{Z_{21} + R_e}\right|^2 + \frac{R_e}{R_S}\left|\frac{Z_{21} - R_S - Z_{11}}{Z_{21} + R_e}\right|^2 \tag{25}$$

where R_e is the resistance connected to the emitter of transistors Q1 and Q2 as shown in Fig. 8 and Z_{11} - Z_{22} are the Z-parameters of the HBT.

From (25) the optimum value of R_S is obtained as;

$$R_{Sopt} = \sqrt{\frac{A + \left(BR_e^2 + R_e\right)\left|\frac{Z_{21} - Z_{11}}{Z_{21} - R_e}\right|^2}{B\left|\frac{Z_{21}}{R_e + Z_{21}}\right|^2 + \frac{R_e}{\left|R_e + Z_{21}\right|^2}}} \tag{26}$$

Fig. 12 shows the reduction in the input referred noise voltage of the Input Buffer with the optimized source resistance.

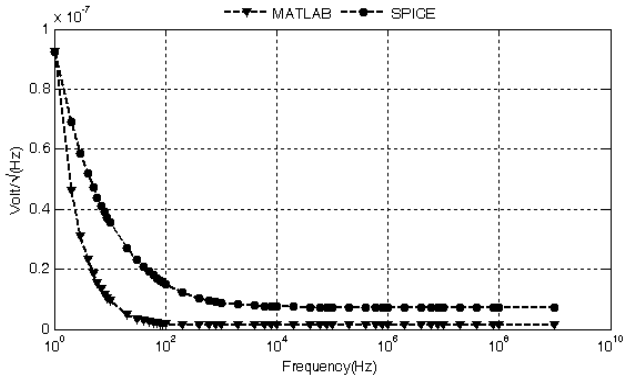

Figure 12: Reduction in input referred noise voltage after optimization

Fig. 12 clearly indicates that both the SPICE simulated and the MATLAB results are almost equal and the low frequency input referred noise voltage is approximately 93 nV/sqrt(Hz). This reduction in the input referred noise voltage improves the SNDR of the THA to 68.34 dB at 3GHz sampling frequency. So, the ENOB is now changed to 11.06 and hence, the resolution is 11-bit which is one bit more than the required resolution of our THA.

Fig. 13 shows the SNDR of the THA both for non-optimized and optimized input referred noise voltage of the Input Buffer. This result is obtained using SPICE at five different sampling frequencies of the THA. It is evident from Fig. 10 and Fig. 12 that with the increase in frequency the input referred noise voltage is getting reduced while Fig. 13 indicates that the SNDR is also getting reduced with increasing frequency. This is because of the parasitic capacitance present in each stage of the THA circuit. To improve the SNDR of the THA with sampling frequency, we have included an inductor in series with R_c of the Input Buffer shown in Fig. 8 to compensate the parasitic capacitive effect.

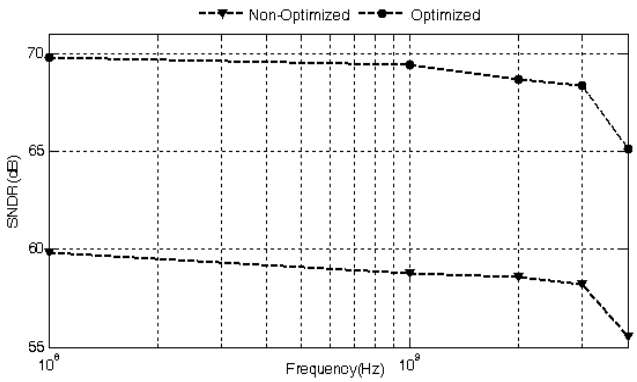

Figure 13: Plot of SNDR of the THA vs. frequency

Fig. 14 indicates the improvement in the SNDR of the THA after inclusion of the inductor. The noise level is not affected much because an inductor is a noiseless component.

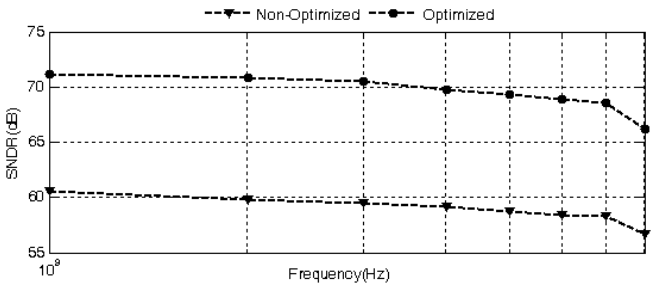

Figure 14: Improved SNDR of the THA vs. frequency

From Fig. 14 it is clear that the SNDR of the THA at 7GHz is 58.31 for non-optimized input referred noise voltage and 68.57 for optimized input referred noise voltage of the Input Buffer and hence an improvement is obtained in the speed of the THA for desired resolution.

VI. CONCLUSION

In this article a computer aided noise analysis technique has been proposed for an Input Buffer which is intended to be used in a THA having a sampling speed of 3GHz and a resolution of 10-bit. Without any noise optimization, it has been seen that the resolution is only 9-bit which is less than one bit from the required resolution of the THA. After the noise optimization of the Input Buffer, the resolution of the THA has been improved by one bit which satisfies our initial consideration of 10-bit resolution. With the inclusion of an inductor in series with the resistor R_c of the Input Buffer, the SNDR and hence the sampling speed of the THA for the required resolution is improved. This computer-aided noise modeling and analysis method can also be applied to other electronic circuits for calculating the input referred noise voltage.

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