Stability Analysis of FPGA –Based Control of Brushless DC Motor Using Fuzzy Logic Controller

Vijaya kumar.M, Gunasekaran.M

Abstract: Slope stability analysis is performed to assess the safe and economic design of a human-made or natural slopes and the equilibrium conditions. The term slope stability may be defined as the resistance of inclined surface to failure by sliding or collapsing. The main objectives of slope stability analysis are finding endangered areas, investigation of potential failure mechanisms, determination of the slope sensitivity to different triggering mechanisms, designing of optimal slopes with regard to safety, reliability and economics and designing possible remedial measures. Successful design of the slope requires geological information and site characteristics for example properties of soil-rock mass, slope geometry, groundwater conditions, alternation of materials by faulting, joint or discontinuity systems, movements and tension in joints, earthquake activity etc. Choice of correct analysis technique depends on both site conditions and the potential mode of failure, with careful consideration being given to the varying strengths, weaknesses and limitations inherent in each methodology. By varying the electrical load, the stability analysis of the brushless dc motor is analysed for various load disturbances and the stability is maintained as shown in hardware implementation.

Keywords: stability, reliability, fuzzy logic controller, voltage, current and speed measurement.

I. INTRODUCTION

Stability analysis of permanent magnet brushless DC motor is designed by using digital pulse width modulation (PWM) technique. Now a day's stability analysis of BLDC motor is very important for various controlling applications. Field programmable gate array (FPGA) technique is used for stability analysis. Due to various disadvantages we designed the stability analysis of brushless dc motor using fuzzy logic controller and digital PWM technique. Before the computer age stability analysis was performed graphically or using hand-held calculator. Today engineers have a lot of possibilities to use analysis software, ranges from simple limit equilibrium techniques through computational limit analysis approaches to complex and sophisticated numerical solutions. The engineer must fully understand limitations of each technique. Fuzzy logic is a form of many-valued logic or probabilistic logic, it deals with reasoning that is approximate rather than fixed and exact. In contrast with traditional logic they can have varying values, where binary sets have two-valued logic, true or false, fuzzy logic variables may have a truth value that ranges in degree between 0 and 1. Fuzzy logic has been extended to handle the concept of partial truth, where the truth value may range between completely true and completely false. Furthermore, when linguistic variables are used, these degrees may be managed by specific functions.

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II.RELATED WORK

We are set the speed of BLDC motor using keypad, A field-programmable gate array (FPGA) is processing the input value and generate pulse width modulation signal, and this PWM signal is covert Analog voltage using DAC(Digital to Analog Converter).

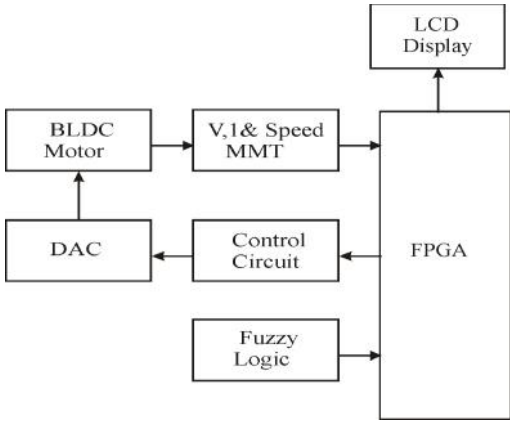


Figure 1.Block Diagram

This DAC Value Control the speed of Brushless DC Motor, and the Voltage, Current and Speed Measurement device measure the Voltage, Current and Speed of Brushless DC Motor, Fuzzy Logic filter the required input, the main use of fuzzy logic is, a lot of input is applied in input port, but we are required some input only so the fuzzy control filtered the exact input from V, I and speed Measurement. The FPGA Control the speed of BLDC motor.

III.BRUSHLESS DC MOTOR

Brushless DC motors (BLDC motors, BL motors) also known as electronically commutated motors (ECMs, EC motors) are synchronous motors which are powered by a DC electric source via an integrated inverter, which produces an AC electric signal to drive the motor; additional sensors and electronics control the inverter output. The motor part of a

brushless motor is often a permanent magnet synchronous motor, but can also be a switched reluctance motor, or induction motor.Brushless motors may be described as stepper motors; however, the term stepper motor tends to be used for motors that are designed specifically to be operated in a mode where they are frequently stopped with the rotor in a defined angular position. This page describes more general brushless motor principles, though there is overlap. Brushless motors offer several advantages over brushed DC motors, including more torque per weight, more torque per watt (increased efficiency), increased reliability, reduced noise, longer lifetime (no brush and commentator erosion), elimination of ionizing sparks from the commutator, and overall reduction of electromagnetic interference (EMI). With no windings on the rotor, they are not subjected to centrifugal forces, and because the windings are supported by the housing, they can be cooled by conduction, requiring no airflow inside the motor for cooling. This in turn means that the motor's internals can be entirely enclosed and protected from dirt or other foreign matter. Brushless motors are more efficient at converting electricity into mechanical power than brushed motors. This improvement is largely due to motor's velocity being determined by the frequency at which the electricity is switched, not the voltage. Additional gains are due to the absence of brushes, alleviating loss due to friction. The enhanced efficiency is greatest in the no-load and low-load region of the motor's performance curve. Under high mechanical loads, brushless motors and high-quality brushed motors are comparable in efficiency. Because the controller must direct the rotor rotation, the controller requires some means of determining the rotor's orientation/position (relative to the stator coils.) Some designs use Hall Effect sensors or a rotary encoder to directly measure the rotor's position. Others measure the back EMF in the undriven coils to infer the rotor position, eliminating the need for separate Hall effect sensors, and therefore are often called senseless controllers. A typical controller contains 3 bi-directional outputs (i.e. frequency controlled three phase output), which are controlled by a logic circuit. Simple controllers employ comparators to determine when the output phase should be advanced, while more advanced controllers employ a microcontroller to manage acceleration, control speed and fine-tune efficiency. Controllers that sense rotor position based on back-EMF have extra challenges in initiating motion because no back-EMF is produced when the rotor is stationary. This is usually accomplished by beginning rotation from an arbitrary phase, and then skipping to the correct phase if it is found to be wrong. This can cause the motor to run briefly backwards, adding even more complexity to the start up sequence. Other sensors less controllers are capable of measuring winding saturation caused by the position of the magnets to infer the rotor position.

IV.FUZZY LOGIC CONTROLLER

Fuzzy logic is a form of many-valued logic or probabilistic logic; it deals with reasoning that is approximate rather than fixed and exact. In contrast with traditional logic they can have varying values, where binary sets have two-valued logic, true or false, fuzzy logic variables may have a truth value that ranges in degree between 0 and 1. Fuzzy logic has been extended to handle the concept of partial truth, where the truth value may range between completely true and completely false. Furthermore, when linguistic variables are used, these degrees may be managed by specific functions. Fuzzy logic allows for approximate values and inferences as well as incomplete ambiguous data (fuzzy data) as opposed to only relying on binary data (binary yes/no choices).Fuzzy logic and probabilistic logic are mathematically similar both have truth values ranging between 0 and 1 but conceptually distinct, due to different inter pretations see interpretations of probability theory. Fuzzy logic corresponds to" degrees of truth", while probabilistic logic corresponds to "probability, likelihood"; as these differ, fuzzy logic we may consider two concepts: Empty and Full. The meaning of each of them can be represented by a certain fuzzy set. Then one might define the glass as being 0.7 empty and 0.3 full. Note that the concept of emptiness would be subjective and thus would depend on the observer or designer. Another designer might equally well design a set membership function where the glass would be considered full for all values down to 50 ml. It is essential to realize that fuzzy logic uses truth degrees as a mathematical model of the vagueness phenomenon while probability is a mathematical model of ignorance. Once fuzzy relations are defined, it is possible to develop fuzzy relational databases. The first fuzzy relational database, FRDB, appeared in Maria Zemankova's dissertation. Later, some other models arose like the Buckles-Petry model, the Prade-Testemale Model, the Umano-Fukami model or the GEFRED model by J.M. Medina, M.A. Vila et al Galindo et al. These languages define some structures in order to include fuzzy aspects in the SQL statements, like fuzzy conditions, fuzzy comparators, fuzzy constants, fuzzy constraints, fuzzy thresholds, linguistic labels and so on.

V.PULSE WIDTH MODULATION

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load. The PWM switching frequency has to be much faster than what would affect the load, which is to say the device that uses the power. Typically switching have to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies. A low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on. The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch.

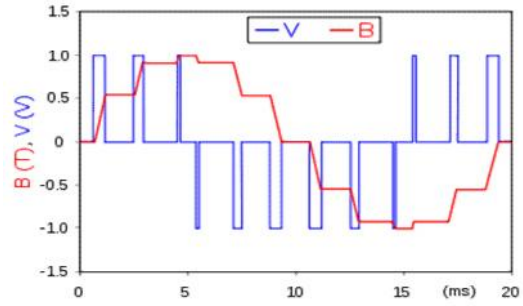


Figure 2.PWM in an AC Motor Drive

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero.

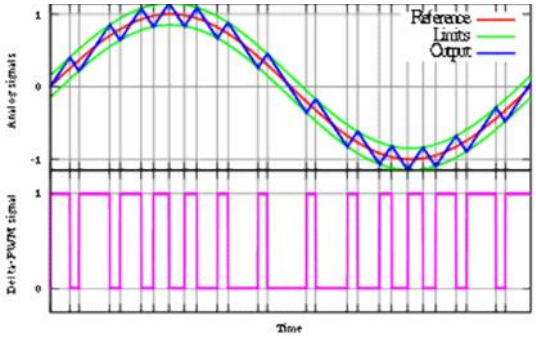


Figure 3.Principle of delta PWM.

The output signal (blue) is compared with the limits (green). These limits correspond to the reference signal (red), offset by a given value. Every time the output signal reaches one of the limits, the PWM signal changes state. The incremented and periodically reset counter is the discrete version of the intersecting method's sawtooth. The analog comparator of the intersecting method becomes integer comparison between the current counter value and the digital (possibly digitized) reference value. The duty cycle can only be varied in discrete steps, as a function of the counter resolution. However, a high-resolution counter can provide quite satisfactory performance. Three types of PWM signals (blue): leading edge modulation (top), trailing edge modulation (middle) and centered pulses (both edges are modulated, bottom). The green lines are the sawtooth waveform (first and second cases) and a triangle waveform (third case) used to generate the PWM waveforms using the intersective method. In telecommunications, the widths of the pulses correspond to specific data values encoded at one end and decoded at the other. Pulses of various lengths (the information itself) will be sent at regular intervals (the carrier frequency of the modulation).The inclusion of a clock signal is not necessary, as the leading edge of the data signal can be used as the clock if a small offset is added to the data value in order to avoid a data value with a zero length pulse.PWM is also used in efficient voltage regulators. By switching voltage to the load with the appropriate duty cycle, the output will approximate a voltage at the desired level. The switching noise is usually filtered with an inductor and a capacitor one method measures the output voltage. When it is lower than the desired voltage, it turns on the switch. When the output voltage is above the desired voltage, it turns off the switch.

VI.FIELD PROGRAMMABLE GATE ARRAY

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing hence programmable. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of a portion of the design and the low non-recurring engineering costs relative to an ASIC design (notwithstanding the generally higher unit cost), offer advantages for many applications.FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together" somewhat like many (changeable) logic gates that can be inter-wired in (many) different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND & XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.Some FPGAs have analog features in addition to digital functions. The most common analog feature is programmable slew rate and drive strength on each output pin, allowing the engineer to set slow rates on lightly loaded pins that would otherwise ring unacceptably, and to set stronger, faster rates on heavily loaded pins on high-speed channels that would otherwise run too slow.

A recent trend has been to take the coarse-grained architectural approach a step further by combining the logic blocks and interconnects of traditional FPGAs with embedded microprocessors and related peripherals to form a complete "system on a programmable chip". This work mirrors the architecture by Ron Perl of and Hana Potash of Burroughs Advanced Systems Group which combined a reconfigurable CPU architecture on a single chip called the SB24. That work was done in 1982. Examples of such hybrid technologies can be found in the Xilinx Zynq™-7000 All Programmable So C, which includes a 1.0 GHz dual-core ARM Cortex-A9 MP Core processor embedded within the FPGA's logic fabric. The flexible nature of programmable logic and its tight integration to the ARM-based processing system offer designers the possibility to add virtually any peripheral they want and create accelerators to extend the performance of the Zynq-7000 devices.

A.FPGA COMPARISONS

Historically, FPGAs have been slower, less energy efficient and generally achieved less functionality than their fixed ASIC counterparts. However, the times are changing. Today's All Programmable FPGAs such as the Xilinx Zynq-7000 and Virtex-7 rival ASIC and ASSP solutions providing significantly reduced power, increased speed, lower BOM cost, minimal implementation real-estate, and maximum on-the-fly configurability. Where previously a design may have

included 6 to 10 ASICs, today the same design can be achieved using only one FPGA. Advantages include the ability to re-program in the field to fix bugs, and may include a shorter time to market and lower non-recurring engineering costs. Vendors can also take a middle road by developing their hardware on ordinary FPGAs, but manufacture their final version so it can no longer be modified after the design has been committed.

B.SECURITY CONSIDERATIONS

With respect to security, FPGAs have both advantages and disadvantages as compared to ASICs or secure microprocessors. FPGAs' flexibility makes malicious modifications during fabrication a lower risk. Previously for many FPGAs, the loaded design is exposed while it is loaded (typically on every power-on). Xilinx programmable devices offer a spectrum of security solutions to designers, ranging from Device DNA and bit stream encryption to Hashed Message Authentication (HMAC) bit stream authentication and specialized security features. Applications of FPGAs include digital signal processing, software-defined radio, aerospace and defence systems, ASIC prototyping, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, computer hardware emulation, radio astronomy, metal detection and a growing range of other areas.FPGAs originally began as competitors to CPLDs and competed in a similar space, that of glue logic for PCBs. As their size, capabilities, and speed increased, they began to take over larger and larger functions to the state where some are now marketed as full systems on chips (SoC). Particularly with the introduction of dedicated multipliers into FPGA architectures in the late 1990s, applications which had traditionally been the sole reserve of DSPs began to incorporate FPGAs instead. Similarly, an I/O pad can connect to any one of the wiring segments in the channel adjacent to it. For example, an I/O pad at the top of the chip can connect to any of the W wires (where W is the channel width) in the horizontal channel immediately below it.Generally, the FPGA routing is unsegmented. This allows chip companies to validate their design before the chip is produced in the factory, reducing the time-to-market. To shrink the size and power consumption of FPGAs, vendors such as Tabula and Xilinx have introduced new 3D or stacked architectures. Following the introduction of its 28 nm 7-series FPGAs, Xilinx revealed that several of the highest-density parts in those FPGA product lines will be constructed using multiple dies in one package.

VII.SIMULTED RESULT

SPEED VARIATION FOR SET-SPEED TO ACTUAL-SPEED

Setting up of speed variation, here we are going to modifying the speed variation by using model sim se 6.3 f. we take the set speed, actual speed and the clock is taken as the input signal. And X4 should be taken as the output. Then these input signals are having its binary value 0 and 1.Among these speed the clock value can also setted and the value between actual value is higher than the set speed value, then output should be maximum to minimum.

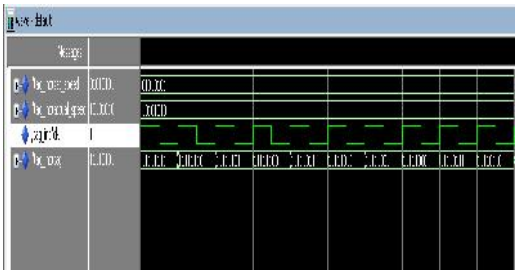


Figure 4.Set Speed to Actual Speed

A) Set speed (X1)
B) Actual speed (X2)
C) Clock (X3)
D) Output (X4)

If the SET speed is lesser than the ACTUAL speed, then the output becomes higher to lower. X1 be the SET speed, X2 be the ACTUAL speed, X3 be the clock and X4 be the output.

X1 = 01010101

X2 = 10101010

X3 = 1

X4 = 11110101

SPEED VARIATION FOR ACTUAL-SPEED TO SET-SPEED

Setting up of speed variation, we take the set speed, actual speed and the clock is taken as the input signal. And X4 should be taken as the output. Then these input signals are having its binary value 0 and 1.Among these speed the clock value can also setted and the value between actual values is lower than the set speed value, then output should be maximum to minimum.

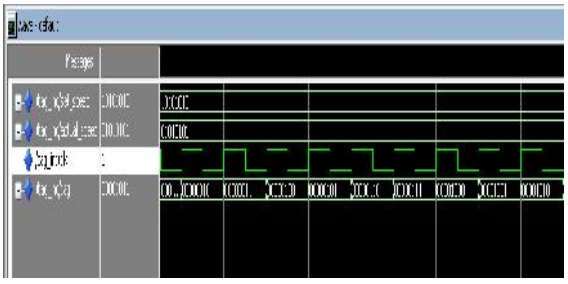


Figure 5.Actual Speed to Set Speed

A) Actual speed (X1)
B) Set speed (X2)
C) Clock (X3)
D) Output (X4)

If the SET speed is higher than the ACTUAL speed, then the output becomes lower to higher. X1 be the SET speed, X2 be the ACTUAL speed, X3 be the clock and X4 be the output.

X1 = 10101010

X2 = 01010101

X3 = 1

X4 = 00001011

SET-SPEED TO ACTUAL-SPEED ARE BOTH EQUAL

Setting up of speed variation, we take the set speed, actual speed and the clock is taken as the input signal. And X4 should be taken as the output. Then these input signals are having its binary value 0 and 1.Among these speed the clock value can also setted and the value between actual value and set speed value are same, then output should be zero.

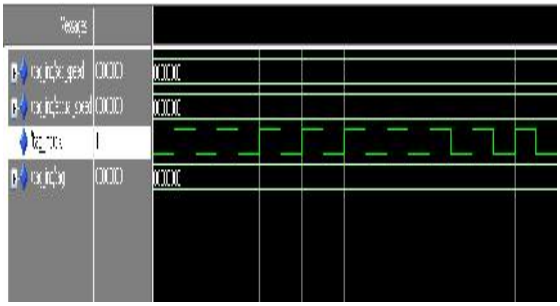


Figure 6. Actual Speed to Set Speed are Equal

A) Set speed (X1)
B) Actual speed (X2)
C) Clock (X3)
D) Output (X4)

If the SET speed is lesser than the ACTUAL speed, then the output becomes equal compared to input setting speed. X1 be the SET speed, X2 be the ACTUAL speed, X3 be the clock and X4 be the output.

X1 = 00000000

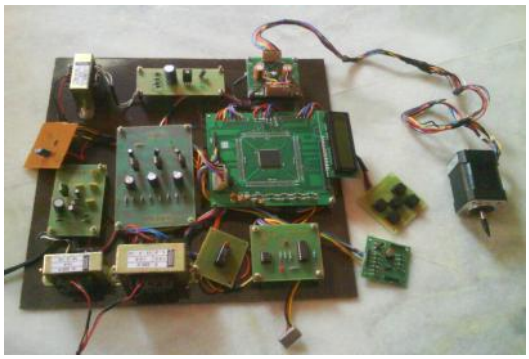
X2 = 00000000

X3 = 1

X4 = 00000000

HARDWARE IMPLEMENTATION

We are set the speed of BLDC motor using keypad, A field-programmable gate array (FPGA) is processing the input value and generate pulse width modulation signal, and this PWM signal is covert Analog voltage using DAC(Digital to Analog Converter).



This DAC Value Control the speed of Brushless DC Motor, and the Voltage, Current and Speed Measurement device measure the Voltage, Current and Speed of Brushless DC Motor, Fuzzy Logic filter the required input, the main use of fuzzy logic is, a lot of input is applied in input port, but we are required some input only so the fuzzy control filtered the exact input from V, I and speed Measurement. The FPGA Control the speed of BLDC motor.

IX.CONCLUSION

Fuzzy control of BLDC machines has several benefits, including simple implementation, requirement of no additional hardware, and not computationally intense. Owing to this simplicity, the technique can be implemented on an FPGA instead of expensive signal processing devices. This paper has discussed the stability issues of digital control strategy for BLDC machines in motoring.It has also investigated the response of the control strategy for sudden changes in load and commanded speed. In order to assess the stability of the proposed control scheme, the system has been analysed using a Lyapunov stability criterion. System response was further evaluated by simulations and verified experimentally for several different operating scenarios.Now days, the analysis of motor is very important in the electrical field. In this project by using the speed control of brushless dc motor, stability is achieved. Sensor based closed loop type operation is designed using fuzzy controller. Thus we have successfully developed the system to analyse the stability of the brushless dc motor using fuzzy controller. This control device can be implemented to any type of motor. The will maintain the desired speed, voltage and current when there is a variation of load. Motor speed can be controlled back to desired value easily. Characteristic of the BLDC motor is also analysed. Thus the stability analysis is made in brushless DC motor.

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