# VHDL Implementation of Switching Type Signal Generation Based on Microblaze in FPGA for Navigation Receiver

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**ABSTRACT: Playing an important role in navigation test, radio navigation generator is widely used in the people/military plane. Traditional equipment composes of analog circuit presents low accuracy and poor reliability. A new kind of digital navigation signal generator is designed in this paper. It receives data and communication from PC by Microblaze embedded soft processor from Xilinx company and demodulated information to control FPGA load different software to generate various navigation signals, which fully meets general radio navigation system test technical requirement by giving full play to the system hardware and software advantages and fulfilling design targets such as the accuracy, flexibility and expansibility.**
**In this a new idea is provided for radio navigation system design and test. This generator can be widely applied for debugging use of people/military plane radio navigation.**

**Keywords—Micro blaze, FPGA, DDS Signal Generator, Synthesized Unit.**

## I. INTRODUCTION

In modern aviation, navigation is an important technology. So far, equipped in almost all the military and civil airports, radio navigation system is the most widely used navigation devices in aviation. At present, radio navigation still has priority in short-range navigation of civilian and military aviation in our country. Also, due to the imperfect landing system device in the existing aircraft, radio navigation system is of vital importance in ensuring safety in planes homing and approaching [1].

In the actual navigation test, to simulate the RF signal of the combined antenna in radio navigation, various signal generators are often designed to satisfy performance of the navigation system and meet technical requirements [2]. Meanwhile, the signal generator must timely adjust signal types, parameters and work modes timely according to the navigation system requirements. Therefore, signal generator must be able to flexibly generate the signals, change its parameters, keep its signal spectrum stabilized and keep its system is reliable.The proposed system adopts Micro blaze soft processor as the control core of generator[3]-[4] for communicating commands with the PC. This can satisfy each requirement in actual application of testing and debugging on navigation. The important role in navigation test, radio navigation generator is widely used in the people/military plane. But traditional equipment composed of analog circuit presents low accuracy and poor reliability.

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A new kind of digital navigation signal generator is designed. It receives data and commands from PC by Micro blaze embedded soft processor of Xilinx
Company and demodulates information to control FPGA load different software to generate various navigation signals, which fully meets general radio navigation system test technical requirements by giving full play to the system hardware and software advantages and fulfilling design targets such as the accuracy, flexibility and expansibility. Therefore, providing a new idea for radio navigation system. This generator can be widely applied to debugging use of people/military plan radio navigation.
The reference paper implements only AM modulation type of testing the navigation receivers.

1. But today's communication systems use a variety of latest digital modulation techniques, hence we have developed two architecture one for analog and other for digital modulations in this project.
2. For realizing the digital modulation have used universal digital modulator for for generating all types of digital modulated signals
3. Signal generator will be designed that contains features that signal can be generating flexibly, the parameters change quickly , signal spectrum stays stability ,and the system is reliable,etc...
4. Fundamentally, characteristics of signal patterns and real time variability are mainly embodied in signal generation technology.
5. This system adopts MicroBlaze soft processor as the central core for generating communicating command with PC and controlling FPGA load differently.

## II. BLOCK DIAGRAM

The figure 1 block diagram consists of sub modules as

1. ADC: For converting analog signals to digital values.
2. RAM: For storing digital values.
3. UART: Serial cable interface for communication purpose.
4. Micro Blaze: It is used for giving the commands.
5. Synthesized Unit: It is used for selecting modulation technique.
6. DDS: It is used for selecting modulation technique.
7. DAC: To convert the digital signal to an analog signal

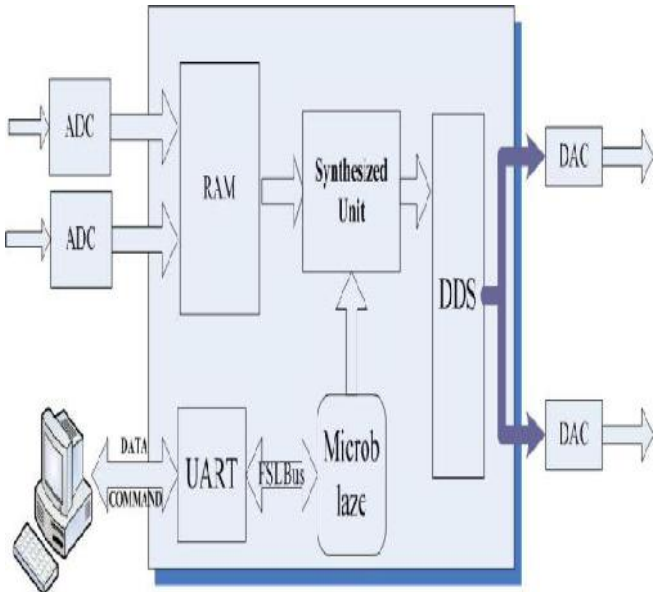


Figure1 processing module for FPGA

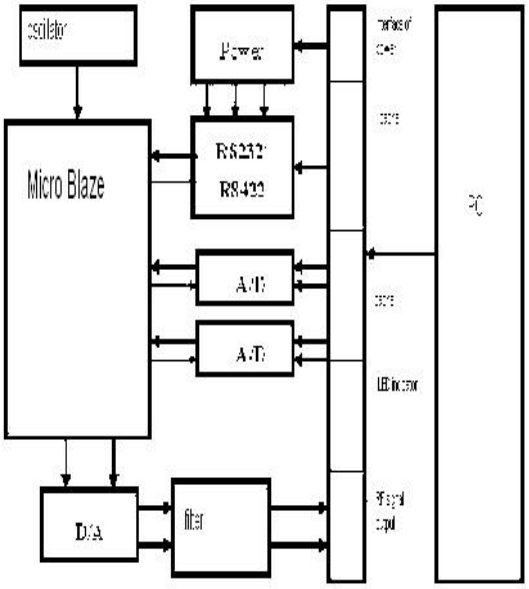


Figure 2 Block Diagram of FPGA

## III. DESIGN SCHEME OF DIGITAL SIGNAL GENERATOR OF RADIO NAVIGATION:

According to different technical requirements of navigation, the generated signal is basically formed by the carrier signal , low frequency modulated signal and an audio modulated signal. Therefore, in this scheme , the signal generator adapts direct digital frequency synthesizer(DDS) technology to design precise clock frequency source, word length of frequency and phase accumulator and sign function table to generate the modulated sign signal whose frequency variation scope, step length change and precision meet the acquirements in the overall design. Large-scaled FPGA is used in this system to realize accurate DDS [6] -[7], ADC converter is used to convert the external signal to be modulated by carrier signal,and the soft embedded processor MicroBlaze communicates with PC by RS422/232 as the control core , figure 1 is the overall scheme of digital signal generator of radio navigation. The contol software of PC wrote in VC6.0 communicates with the generator through RS422/232 is in charge of transmitting control command to set frequency, Azimuth angle,channel,working mode and other parameters of navigation signal and receiving status and data of the generator after every change.In this system, as a master unit MicroBlaze sents parameters to FPGA after demodulating data from PC while FPFA generates accurate navigation signal to high speed DAC converter as the ground floor synthesis unit.Meanwhile, multiple clock signal used in the system are generated in phase lock logic part of FPGA from external oscillator.

**Direct Digital Synthesizer:**

A Direct Digital frequency synthesizer (DDS) design and prototype suitable for space-borne applications are presented. The design is targeted for use in the uplink section of the RF subsystem of the New Horizons Pluto spacecraft currently under design at APL. Design and analysis of the digital portion of the DDS are presented along with experimental data from the prototype system, discrete digital to analog converter.

Direct Digital frequency Synthesizers (DDS) are a common component in a variety of communication systems, especially those requiring fast frequency hopping, low power dissipation, and small form factor.A DDS at its simplest is a clock-dividing counter, termed the phase accumulator, which generates a digitized ramp wave form.This ramp is converted to a sign wave representation and subsequently translated into the analog domain by a digital to analog converter (DAC).Subsequent filtering of DAC output can be used to remove the high frequency component that arise from the data conversion process**.** Figure 3 illustrates the conceptual system with a j-bit accumulator output truncated to a k-bit ROM Address space and a m-bit DAC. DDS performance is measured in a number of ways. Some are fairly generic, including power dissipation and maximum input clock rate and output frequency .Others are more specific , relating to minimum step size and the spectral purity of the DDS output. The DDS output spectrum reflects the fact that a DDS effectivly samples a sign wave output.As a result inaccuracies due to finite word length effects as well as Nyquist sampling consideration cause the output spectrum to contain energy at frequencies other than the fundamental.These peaks,termed spurs, determine the level of the DDS ,which is defined as the Spurious Free Dynamic Range(SFDR).Non-idealities in the DAC can futher degrade the SFDR as well.In general,peaks which are closer in frequency to the fundamental present move problems than peaks further out ,simple because they are more difficult to attenuate with an output low pass filter.

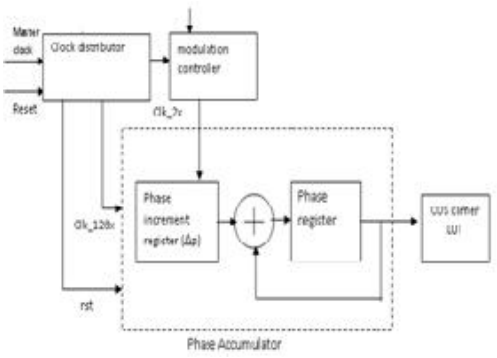


Figure 3 Direct Digital Synthesizer

**Implementation of DDS**

In this figure 3 we are using direct digital synthesizer for generation of the carrier signal.All we know about that by using DDS we can generate a carrier signal in the form of sine or cosine or sinecosine.Xilinx itself generate the code for DDS i.e IP core generations.In that we should select the options about the carrier or signal frequency in MHZ and phase off set and data width and phase increment register,data width depends on data width or we can have a option like programmable then we can give the phase of set and frequency levels through the programme and we are taking the carrier signal from the DDS and we do the modulation like AM,FM,QPSK and BPSK.And in FM technique we are taking DDS signal as the message signal and we are generating the carrier by using hareware description language.

**ADC**

The analog to digital module converter word (the AD1) converts signal at a maximum sampling rate of 1 million samples per second,fast enough for the most demanding audio applications.The AD1 uses a 6 –pin header connector, and it a less than one square inch is small enough to be located at the signal source.

**1. Features include :**

**.**Two ADC's 7476MSPS 12-bit A/D convertor chips.
**.**A 6-pin header connector
**.** A 6-pin connector
**.**Two 2-pole sallen-key anti-alias filters
**.**Two simultaneous A/D conversion channels at upto one Msa per channel
**.**Very low power consumption
**.**Small form factor(0.955''x0.80'').

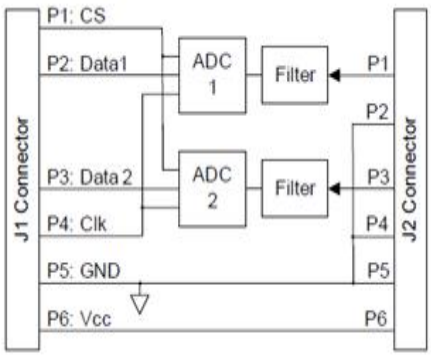


Figure4 Block Diagram of ADC

**1. Functional description:**

The figure 4 AD1 converts an analong input signal ranging from 0-3.3 volts to a 12bit digital value in the range 0-4095.The AD1 has two simultanious A/D channels ,each with a 12-bit converter and filter .Each channel can sample a separate stream of analog signals.The AD1 can also convert a signal stream of analog signals using only one channel.Each channel has two 2 –pole sallen-key anty alias filters with poles set to 500 KEYHz.The filters limit the analog signal bandwidth to a frequency range suitable to the sample rate of the converter.The AD1 uses the SPA/MICROWIRE serial bus standard to send converted to the host system.The serial bus can run at upto 20 MHz.The AD1 has a 6-pin header and a 6-pin connector for easy connection to a digilent system board or other digilent products .Some system boats ,like the digilent Pegasus board,have a 6-pin header that can connect AD1 with a 6-pin cable.To connect the AD1 to other digilant system boats a digilent Modular Interface Board(MIB) and a 6-pin cable may be needed.The MIB plugs into the the system board, and the cable connects the MIB to the AD1.The AD1 can be powered by voltage from either a digilent system board or an outside device.Damage can result if power is supplied from both sources or if the outside device supplies more than 3V.

**DAC**

The Digilent pmodDA2 Digital to AnalogConverter module,converts signals from digital values to analog voltages on two channels simultaneously with twelve bits of resolution. The pmodDA2 uses a 6 pin header connector and,at less than one square inch, is small enough to be located where the reconstructed signal is required.

**1. Features include:**

**.** Two National Semiconductor DAC121S101, 12-bit D/A converters
**.** A 6-pin header and a 6-pin connector
**.** Two simultaneous D/A conversion Channels.
**.** Very low power consumption
**.** Small form factor(0.80''x0.80'').

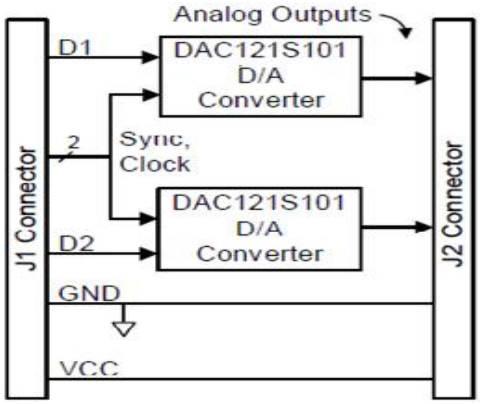


Figure 5 DAC Block Diagram

The pmodDA2 can produce an analog output ranging from 0-3.3 volts when operated with a 3.3V power supply. It has two simultaneous D/A conversion channels, each with a 12-bit converter that can process separate digital signals. The pmodDA2 is equipped with two DAC121S101 digital to

analog converters.Sending commands via the SPI/MICROWIRE serial bus to the D/A convertors produces outputs. The two converters are connected in parallel so that commands are sent both converters simultaneously. The PmodDA2 is designed to work with either Digilent programmable logic system boards or embedded control system boards. Most Digilent system boards, such as the Nexys, Basys, or Cerebot, have 6-pin connectors that allow the pmodDA2 to plug directly into the system board or to connect via a Digilent six-wirecable some older Digilent boards may need a Digilent Module Interface Board (MIB) and a 6-pin cable to connect to the PmodDA2.The MIB plugs inti the system board and the cable connects the MIB to the PmodDA2.

See Table 1 for a description of the signals on the interface connectors J1 and J2

**Table 1: Interface Connector Signal Descriptions**

| | |
|---|---|
| **Digital Interface – J1** | |
| 1 | SYNC (common) |
| 2 | DINA (converter IC1) |
| 3 | DINB (converter IC2) |
| 4 | SCLK (common) |
| 5 | GND |
| 6 | VCC |
| Analog Interface – J2 | |
| 1 | VOUTA (converter IC1) |
| 2 | N/C |
| 3 | VOUTB (converter IC2) |
| 4 | N/C |
| 5 | GND |
| 6 | VCC |

The PmodDA2 is usually powered from the Digilent system board connected to it.The power and ground connections are on pins five and six of the digital interface connector J1. Alternatively, the PmodDA2 can powered from an external power supply provided through pins five and six of the analog interface connector J2.In this case the power select jumper on the system board should be set to disconnect power from the system board to J1.Damage may result if two power supplies are connected at the same time. The Digilent convention is to provide 3.3 V to Pmod modules. The PmodDA2 can be operated at any power supply voltage between 2.7 V and 5.5V, however caution should be exercised if using any voltage between 2.7V and 5.5V. However caution should be exercised if using any voltage greater than 3.3V, as damage to the Digilent system board could result.

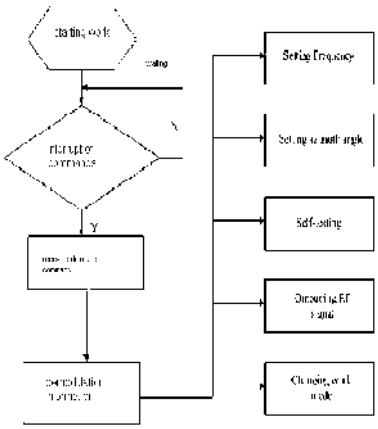

Figure 6 Software flow of MICROBLAZE

**Implementation of MICROBLAZE:**

In our project the MicroBlaze place a main important role. It is a soft core processor. And we know about the two types of processors, those are MicroBlaze and the Power PC is,MicroBlaze is a soft core processor and the power PC is hard core processor.

**MicroBlaze:**

Which is a soft core processor, the same part of the FPGA will act as a microblaze processor by implementing the hardware description language means by the vhdl code we are making act of FPGA as MicroBlaze.So it is called as soft core processor. No need of any external hardware circuitry.

**Powered PC:**

It is a hard core processor,means it is different than microblaze. In this we should require the external hardware by connecting the external hardware of the power PC to FPGA we can use the processor. Then the circuit complexity may increase.

So in this project we are implementing MicroBlaze soft core processor only. And this processor will take the information from the PC by using UART.So we receive the commands in HEXA,ASCII format.By using these commands only we can change our parameters of modulation techniques like setting frequency, setting azimuth angle, changing work mode, self testing and output coding.According to these commands the modulation techniques are selected in the synthesized unit.

## IV SIMULATION RESULTS:

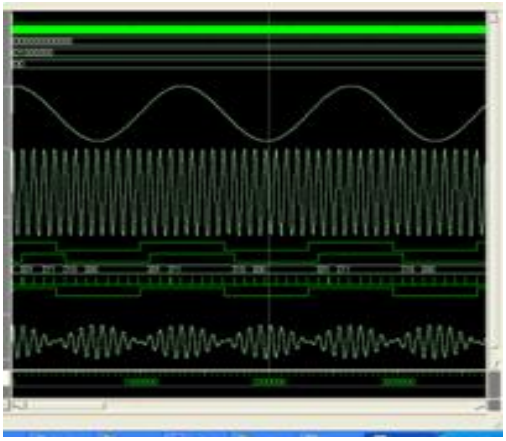

Figure 7 Simulation of AM

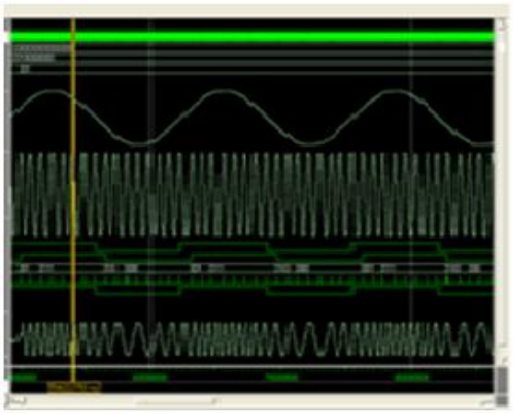

Figure 8 Simulation of FM

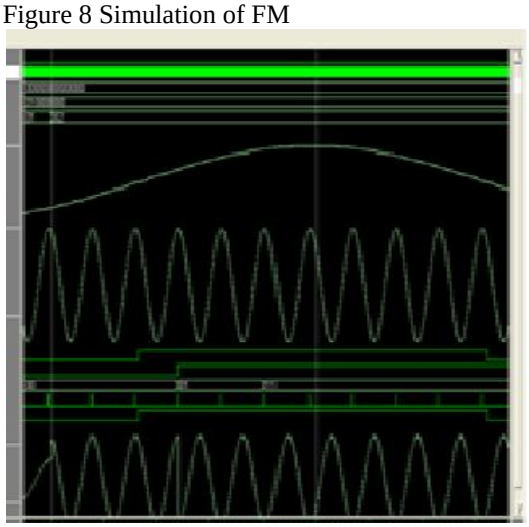

Figure 9 Simulation of BPSK

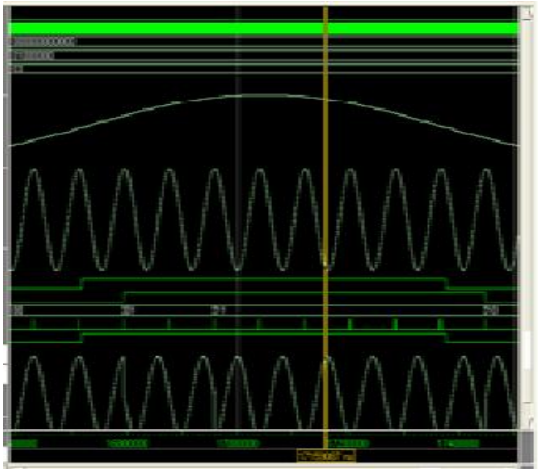

Figure 10 Simulation of QPSK

**V CONCLUSION:**

In this paper, the digital signal generator of radio navigation is implemented by soft processor MicoBlaze whose key portion is achieved in a single FPGA chip, which overcomes the disadvantage of low accuracy and flat tuning in a traditional method. Simultaneously, various kinds of signals can be loaded in this system, obtaining more flexibility and better expandability. AM, FM, BPSK and QPSK modulation technique have been done. Through the numerical test and simulation results, the veracity and precision is conformed. Favorable results have been acquired in practical application.

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