Analog to Digital Converter (ADC) Review

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Abstract: This paper presents basic introduction about analog to digital conversion process. This is done by two steps: Sampling and Quantization. During the conversion process some parameters are more important such like resolution, SNR, SFDR which are introduced in to this paper. The performance of the ADC is measured by INL, DNL and quantization error which are also defined. There are different types of ADCs which are also introduced using with some literature regarding to this analog to digital conversion.

Keywords: Analog to Digital converter (ADC), pipeline, sample and hold, Digital to Analog converter (DAC), CMOS.

I. INTRODUCTION

Generally the data available from real world are in analog form, but this analog data storage procedure is more complex compare with digital storage. There is also more advantage like digital data storage requires less memory compared to analog data, less noisy and provides good encryption & security features [4], [19]. Therefore we required the analog to digital converter (ADC). Hence ADC plays an essential role in all kinds of electronics systems. As we know digital signal processing (DSP) is more popular today in this case ADC is required because of requirement of digital data only. Using this feature it is very popular in very large scale integration (VLSI). Analog to digital converters are useful building blocks in many applications such as data storage read channel [1] and an optical receiver [2] because they represent the interface between the real world analog signal and the digital signal processors. Recently digital multimedia application is more popular in this case ADC is required. In LED & LCD displays digital data is also required [5].

II. HOW TO CONVERT AN ANALOG SIGNAL IN TO DIGITAL SIGNAL

ADC is a device that uses sampling to convert continuous time signals in to discrete digital form. [4] ADC is such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. [3], [21] This process is done by two steps: Sampling and Quantization. Digitizing the coordinate value is called sampling and digitizing the amplitude value is called quantization. Sampling does the breaking down the analog value in to set of discrete values & quantization takes only a few discrete values from the available value and converting this discrete value into the digital values through the encoding process.

[5] For example, we have 0-8V peak-to-peak signal. Separate them into discrete states with 2V range for each state, so that we have 4 different quantization levels as shown in to the table and corresponding assign the digital value for each quantization level.

TABLE : I Quantization and Encoding for different voltage range

Voltage range(V)	Quantization levels	Encoding
0 – 2	1	00
2 – 4	2	01
4 – 6	3	10
6 – 8	4	11

Sampling frequency for the conversion process as per the Nyquist rate is at least twice of the maximum frequency of the input analog signal for the faithful reproduction of the input signal. For example, input signal is [3], [21-22]

$$X(t) = A\cos(2 * \pi * fm * t) \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where, fm is the input signal frequency, then the sampling frequency is fs = 2*fm as per the Nyquist rate [19].

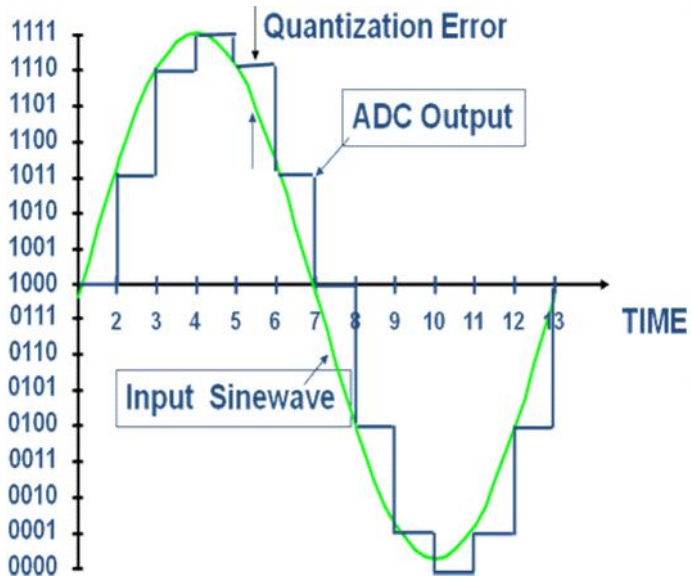

Fig. 1. Sampling and Quantization [4]

This figure shows 4-bit (16 level) ADC sampling a sine wave input analog signal in to digital signal. Digital data may have any value from its 16 level.

III. ADC PARAMETERS

There are several parameters are used to test the performance of the conversion process.

A. Resolution

The resolution of the converter indicates the number of discrete value it can produce over the range of analog values [6-8]. It is usually expressed in bits. [20] For example, ADC

with a resolution of 8-bits can encode an analog input to one in 256 different levels, because of 2^8 = 256. It ranges from 0 t0 255 or -129 to 127. Resolution can also be defined electrically, and expressed in volts. The resolution Q of the ADC is equal to the least significant bit (LSB) voltage [5],

$$Q = \frac{V_{high} - V_{low}}{2^m - 1} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Where, m = resolution in bits

[5] For example, $X(t) = A\cos(t)$ where A = 5V. It swings from -5 to 5 volts. If ADC resolution is 8 bits: 2^8 – 1 = 255, and hence Q = (10 - 0) / 255 = 39mv. Resolution of converter is limited by the signal-to-noise ratio (SNR) that can be achieved for a digital signal.

B. Signal to noise ratio (SNR)

SNR is most important parameter of the ADC. It measures the signal power and noise power for the output digital signal and give the amount of signal is distorted [3-4], [6]. So that high SNR is acceptable.

C. Total harmonic distortion (THD)

During the conversion process some samples are mixed due to noise and generate distorted signal. It is caused by ADC non-linearity, which generates harmonics of the input signal; it is undesired at the output stages [6], [25]. So that THD gives amount of harmonics are generated in to digital signal. It is measured in db as sown in to the figure 2.

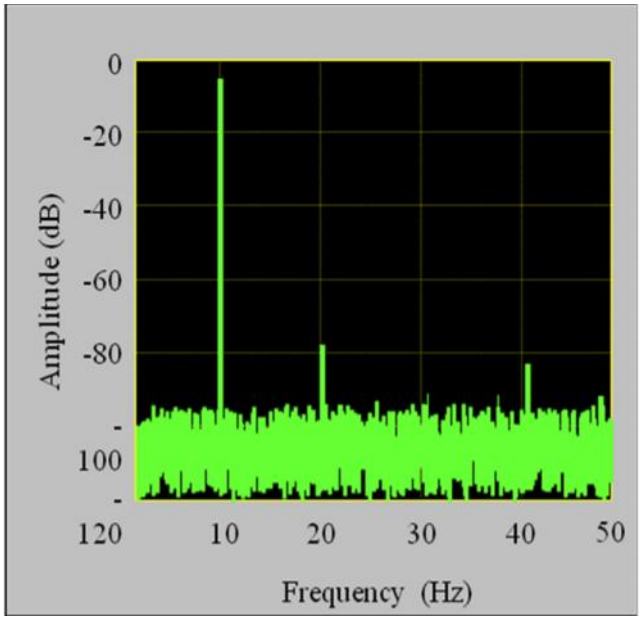

Fig. 2. Total harmonic distortion [6]

D. Spurious free dynamic range (SFDR)

Dynamic range is a range for which output follows to input as per the requirements. After a sometime harmonics are generated due to non-linearity, so that the operating ranges for which spurious response are minimal is called the spurious free dynamic range [6], [25]. SFDR is always given at a particular frequency as shown in figure 3. It is the difference between primary and next highest spur as shown in to the figure 3.

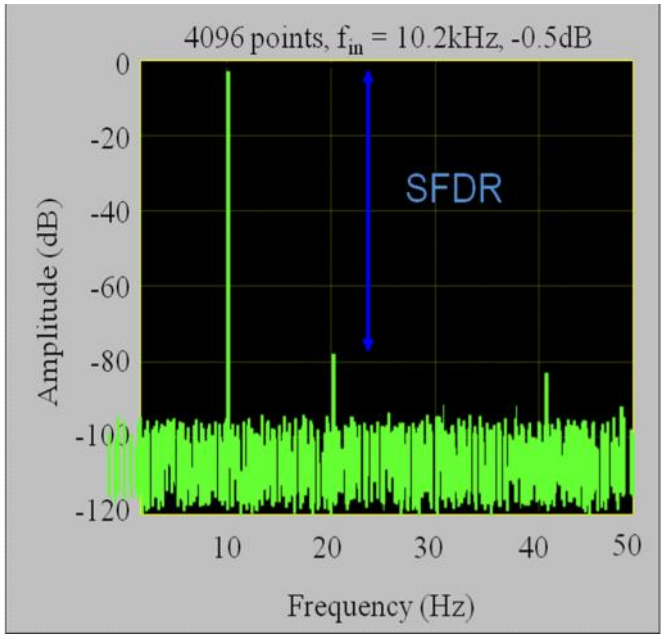

Fig. 3. Spurious free dynamic range [6]

E. Power dissipation

It gives amount of power dissipated by a specific ADC. Less the ADC circuit area less the power consumption [3], [22]. So that fabricates the ADC by the CMOS technology to cover less area.

IV. ADC ERRORS

There are several errors are generated during conversion process as like:

A .Aliasing

If input signal is changing much faster than the sampling rate, then the digital signal reconstruction of the analog signal is not same as original one, but some spurious signal is generated is called aliases. This problem is called aliasing. [5] For example, 2 KHz sine wave being sampled at 1.5 KHz would be reconstructed as a 500Hz sine wave. To avoid aliasing, an input signal to an ADC must be low-pass filtered to remove frequencies above half of the sampling rate. This filter is called anti-aliasing filter [6]. Aliasing error is shown in to the figure 4.

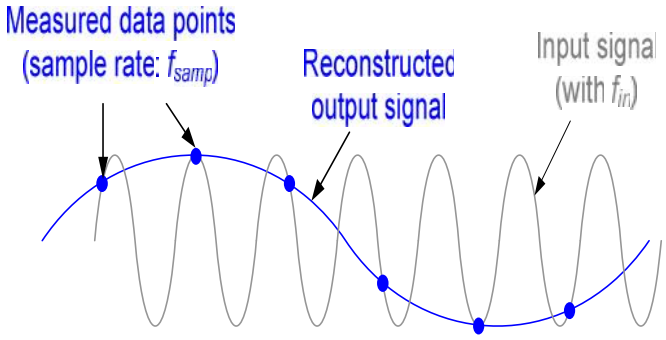

Fig. 4. Aliasing [7]

B. Quantization error

Quantization error (quantization noise) is the difference between the original signal and the digitized signal as shown in figure 5 [4], [5]. Hence the amplitude of the error at the sampling instant is between zero and half of one LSB $(\pm 1/2LSB)$. It is due to the finite resolution of the digital signal and it is an avoidable in all types of ADCs. This error is intrinsic to any types of ADCs. It is reduce by higher resolution of ADC [6].

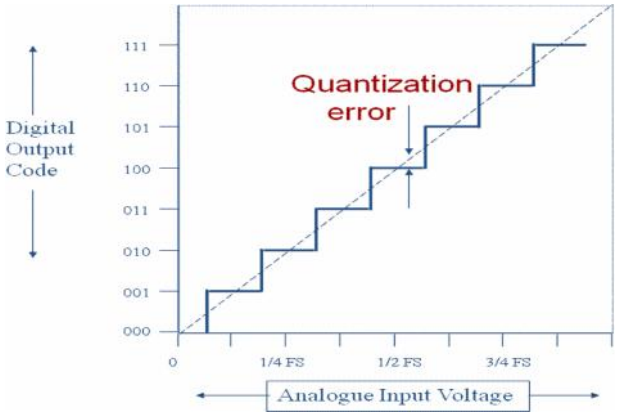

Fig. 5. Quantization error [7]

C. Non-linearity

All ADCs suffer from non-linearity errors caused by their physical imperfections, causing their output to deviate from a linear function of their input. These errors can be mitigated by calibration techniques or prevented by testing. [5] A Non-linearity error reduces the dynamic range of the signals, also reducing the effective resolution of the ADC. This error is intrinsic to any type of ADCs. The most important parameters for linearity are Integral non-linearity (INL) and Differential non-linearity (DNL).

I. Integral non-linearity (INL)

It is the maximum deviation between an actual code transition point and its corresponding ideal transition point. INL is measured in LSBs, and calculated after offset and gain errors have been compensated [6], [25]. A positive INL indicates transition occurring later than ideal and negative INL means transition earlier than ideal [7]. It is measured in LSBs.

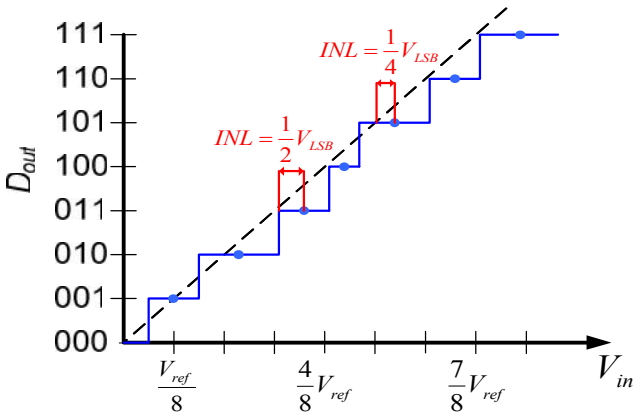

Fig. 6. Integral non-linearity [7]

II. Differential non-linearity (DNL)

It is measure of the maximum deviation from the ideal step size of 1 LSB. Results in narrow or wider code widths than ideal and can result in missing codes [6], [25]. DNL error is measured in LSBs [7].

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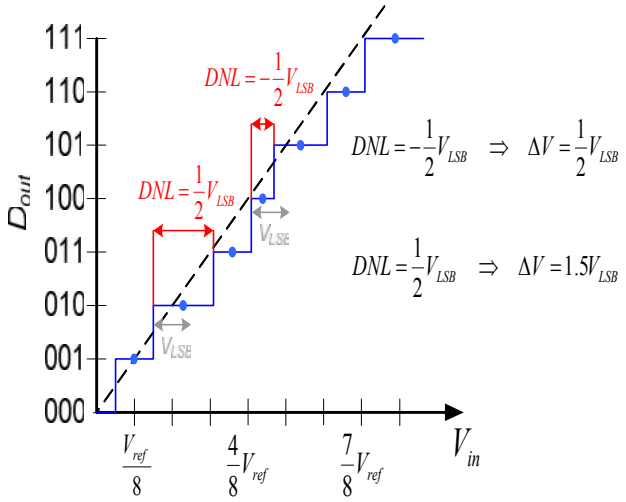

Fig. 7. Differential non-linearity [7]

D. Aperture error

It is generated by a clock jitter and it is generated when digitizing a time variant signal. Imaging a sine wave signal, $X(t) = A\sin(2*\pi*f0*t)$ provided that the actual sampling time uncertainty due to the clock jitter is dt, error can be estimated as [5],

$$dt < \frac{1}{2^q * \pi * f0} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Where, q = no of ADC bits.

The error is zero for DC, small at low frequencies, but significant when high frequencies. Clock jitter is caused by phase noise.

V. TYPES OF ADCs

There is a different way to implement an electronic ADC device is shown below:

A. Direct conversion or Flash ADC

It has a bank of comparators sampling the input signal in parallel. The comparator bank feeds a logic circuit that generates a code for each voltage range as shown in figure 8. It takes input parallel and as per the input voltage, comparator generates logic code and these logic codes are converted in to digital data by an encoder [8], [10]. Direct conversion is very fast, capable of gigahertz sampling rates, but only 8 bits of resolution, since the no of comparators needed 2^n – 1, doubles with each additional bit, requiring a large & expensive circuit [23]. It has large die size, a high input capacitance and high power dissipation. They are used for video, ultra wideband communication or other fast signals in optical storage, disk drivers, cable modems, CCD image systems, digital video and fast Ethernet systems [9]. They are used when a high sampling rate is required doesn't matter about high resolution.

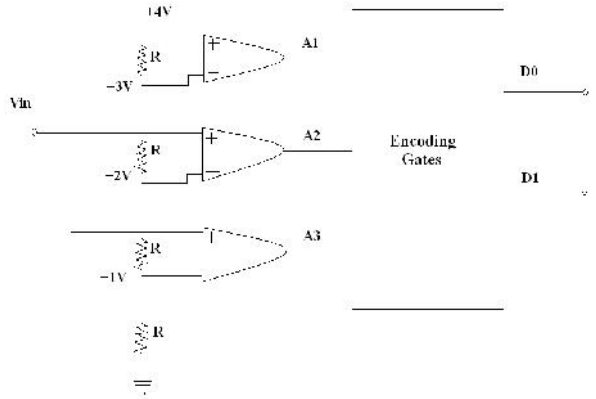

Fig. 8. Flash ADC Architecture [8]

Flash ADC is limited by only a few number of bits of resolution up to 8-bits because of the complexity of the circuits. [9] In a flash ADC the comparator only needs to be low offset and to resolve its input to a digital level; there is no linear settling time involved. Some flash converters require preamplifiers to drive the comparators. [10] Mohamed Shaker suggests a low power 1-GS/s 6-bit CMOS flash ADC. This design requires only few no of comparator and multiplexer to generate the required binary code. Using this multiplexer no of comparator is required less. This architecture can be extended to high resolution applications because of the simplicity of the circuit.

There is also solution for lower bits of resolution, with the use of two-step flash ADC. In two-step flash ADC conversion is done by two steps one is coarse flash ADC (MSB) and another is fine ADC (LSB). [25] In this case increse the no of bits of resolution and decrease the no of comparator is required from 2^n - 1 to 2(2^n/2 - 1), so that power consumption is also decrease and increase the ADC performance. Hence this process is very easy and in future it is used for high resolution application. [11] Aamir Zjajo suggests a low power, low voltage for two step ADC. It uses a time interleaved sample and hold circuit along with 5-bit coarse ADC and 8-bit fine ADC. The 8-bit of fine ADC are generated with sufficient accuracy without using compensation by using a folding and interpolating ADC.

B. Successive Approximation ADC (SAR)

It uses a comparator to successively narrow range that contains the input voltage. [7-8], [25] At each successive step, the converter compares the input voltage to the output of an internal digital to analog converter (DAC). At each step in this process, the approximation is stored in a successive approximation register (SAR). As shown in figure 9 input analog voltages Vin is given to comparator, during the first clock pulse low-to-high transition, the MSB Q7 of the SAR is set. Then DAC generate analog equivalent voltage to Q7 bit, which is compared to Vin. If the comparator output is low, it means the DAC output Va>Vin, then the SAR clear its Q7 bit and set Q6 bit. If the comparator output is high, the DAC output Va < Vin then the SAR will keep the MSB Q7 set. This process is continue until both are equal Va = Vin. At that time SAR forces conversion complete & enable latch, so it takes data parallel as shown in figure 9.

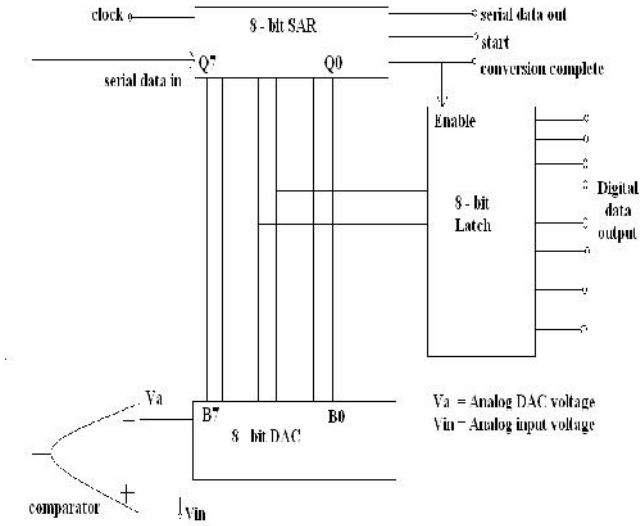

Fig. 9. SAR ADC Architecture [8]

In a SAR converter comparator determines one bit at a time from the MSB down to the LSB. This serial nature of the SAR limits its speed to no more than a few mega-samples per second (MSPS). SAR converters are available in resolution up to 16-bits. The slower speed also allows the SAR ADC to be much lower in power consumption. [12] This paper presents 1-V 8-bit 50 KS/s successive approximation analog to digital converter implemented in 1.2 µm CMOS. It is based on inverting op-amp configuration with biasing current added to the op-amp negative terminal.

C. Wilkinson ADC

It is based on the comparison of an input voltage with that produced by a charging capacitor. The capacitor is allowed to charge until its voltage is equal to the amplitude of the input pulse. Then the capacitor is allowed to discharge linearly, which produces a ramp voltage. At the point when the capacitor begins to discharge, a gate pulse initiated. The gate pulse remains on until the capacitor is completely discharged.

Thus the duration of the gate pulse is directly proportional to the amplitude of the input pulse [5], [24]. These ADC has the best differential non-linearity (DNL).

D. Pipeline ADC

It uses two or more steps of sub ranging. First coarse conversion is done. In a second step, the difference to the input signal is determined with a digital to analog converter (DAC)[5], [14]. This difference is then converted finer, and the results are combined in a last step, as shown in figure 10. By combining the merit of the SAR & FLASH ADCs this type is fast, has a high resolution and only requires a small die size. Generally for high resolution and high speed this ADC is used. [25] A pipeline ADC employs a parallel structure in which each stage works on to a few bits of successive samples concurrently. This design improves speed at the expense of power and latency, but each pipelined stage is much slower than flash section.

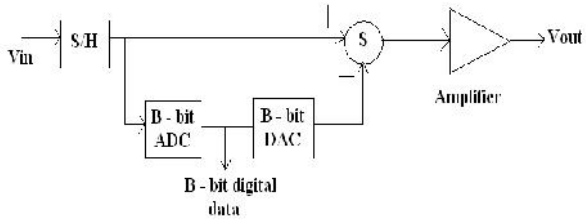

Fig. 10. Pipeline ADC Architecture [14]

[13] The pipeline ADC requires accurate amplification in the DACs and interstage amplifiers, and these stages have to settle to the desired linearity level. Pipeline architecture provided resolution from 8 to 14 bits. [14] This paper presents capacitor error-averaging technique, updated with look-ahead decision and digital calibration for 14-bit pipeline architecture. This work achieves by using error-averaging amplifiers to eliminate errors resulting from capacitor ratio mismatch. [15] This paper presents a high speed single-channel pipeline ADC sampling at 2.4 GS/s. the high sampling rate is achieved through the use of fast open-loop current-mode amplifiers and the early comparison scheme.

There is also a time interleave architecture is used in which N different track-and-hold circuit is used along with N sub-ADCs are used. [16] Time interleaved architectures suffer from three impairments: offset, gain, phase skew mismatch between the banks of sub-ADCs. In this case N different clock phase generators are needed. Hence these are very complex process, so that different technique is used. [17] Sandeep and Michael suggest time interleaved architecture that eliminates the need to correct timing offsets and is scalable to high sampling rate. To eliminate timing skews, a Nyquist rate sampling switch is used, which is followed by subsampled, double-sampled time-interleaved sample and hold stages.

VI. CONCLUSION

Analog to digital conversion are reviewed in this paper using various techniques such as: flash or direct conversion, successive approximation, Wilkinson, pipeline, two-step, time-interleaved architecture. These different methods are used as per the requirement for the high speed, high resolution, less area, low power dissipation, low voltage etc. Some reference papers are listed below for more information.

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