Dynamically Reconfigurable Control Structure for Asynchronous AC Drives

M.Sathish Kannan and S.Vasantharathna

A*bstract*— **In this paper describes about the design of Field Programmable Gate Array based space vector pulse width modulated voltage/frequency (SVPWM-V/F) scalar control system for three phase induction motor drive. The SVPWM-V/F Control algorithm is designed in a matlab/simulink environment using Xilinx system generator blocksets (XSG). Design of FPGA based motor control will be much competent when compared to DSP and microcontroller based motor control. The advent of FPGA implementation of SVPWM-V/F control system will be minimized Total Harmonic distortion in the output voltage and current of voltage source inverter. It also gives efficient usage of supply voltage when compared to sinusoidal modulation techniques and reduces audible noise, increases global motor reliability. The above system is implemented on the Xilinx SPARTAN-3 XC3S400 FPGA development board. Simulation and experimental results are presented to validate the performance of proposed system.**

Index Terms — **Field Programmable Gate Array (FPGA), Space Vector PWM (SVPWM), Xilinx System Generator (XSG), Voltage Source Inverter (VSI), Induction Motor (IM).**

I. INTRODUCTION

The rapid increase in the field of power electronics-drives and their industrial applications, such as robotics, smart home appliances, automotive, aircraft, space research demands energy efficient and highly accurate digital controllers. It also demands low cost controller with fully integrated and multitasking control facility. It requires sophisticated control algorithms which can give higher performance and the ability to adapt the environment by changing the control strategy and control parameters. It should be fast enough for real time computation and produce accurate, reliable results and safety even in harsh environment. A robust solution is needed to satisfy the control requirements. Digital solutions such as Microcontrollers, DSP and FPGA play a dominant role in the area of control system implementation platform. Today many of the complex control algorithms are systematically implemented using software based digital controllers such as DSP.

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The limitation of DSP based controller is its fixed internal architecture. It runs in serial fashion which increases the execution time of system which is having complex control Algorithm. This introduces delay in control closed loop which affects the control bandwidth of the system. In time critical applications like aircraft control, radar applications where high control quality and large bandwidths are bottlenecks. In industrial applications, high control performance is achieved with the help of FPGA. It is evident from the various researches carried out in this area [1-2]. FPGAs are digital IC that contain programmable logic blocks along with interconnect switches to control the logical blocks. Dynamically reconfigurable control structure and parallelism is the major strength of FPGA .It offers programmers to configure and design for their versatile needs and tasks in digital hardware platform.

A digital hardware platform is offered by FPGA on which a programmer can verify their physical implementation of new algorithm. It is used to develop prototype application specific intellectual circuit (ASIC) design. A FPGA prototype involves various steps the first step is to develop a functional simulation, and emulation. Based on the simulation results then finally prototyping the physical system [3].

1.1 Advantage of FPGA based motor control:

Motor control systems are the heart of industrial applications such as robots, automobiles, automated guided vehicles, home appliances like washing machines, refrigerator, Dryer. The most popular types of motor used in these applications are Permanent magnet synchronous motor (PMSM), Induction motor (IM), Stepper motor, Brushless Dc motor (BLDC). Induction motor control is a highly nonlinear time varying parameter application that demands large amount of computing power due to fast dynamics of current flow in the motor and power electronics switches. According to the U.S Department of energy, using power electronics converter based variable speed motor drives in washing machines can save up to 140 KWh per year [4].The quality of the system design in terms of energy consumption, cost effective, safety, high performance and to satisfy customer requirements. The FPGA Based motor control system is satisfying all these requirements to increase performance of the overall system. It can also help system designers create greener products to get energy star rating certification [5].

2. Principle of space vector modulation:

space vector pulse width modulation is quite different from other pwm methods. In SVPWM the inverter treats as a single unit, it can be driven to eight unique states as shown in Table. Modulation is achieved by switching the state of the inverter. SVPWM is a digital modulating technique; it can be easily implemented into digital system. The objective of it's to generate PWM load line voltages that are average equal to reference load line voltages. This is done in each sampling period by properly selecting the switching states of the inverter and calculate appropriate time period for each state.

The selection of states and their time periods are achieved by space vector transformation.

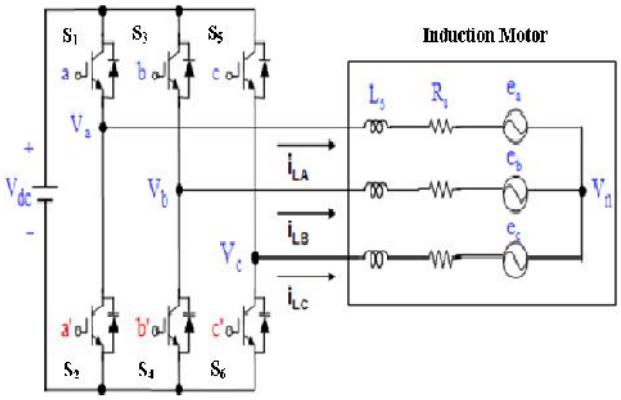

Fig.1. Three phase diode clamped two levels Voltage source inverter

The circuit shown in Fig.(1) is Two level Diode clamped - Three phase voltage source inverter. It has six power electronic switches(S_1-S_6) that shape the output, which are controlled by the switching variables a, a', b, b', c, c' when an upper transistor is switched on, the corresponding lower transistor is switched off, Depending on the switching combination ,the inverter will produce different output voltage, creating two level signal [6-8].

The relationship between the switching variable vector $[a,b,c]^t$ And line - to - line voltage vector $[V_{ab},V_{bc},V_{ca}]^t$ is given by the equation (1)

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1)$$

Also the relationship between switching variable vector $[a,b,c]^t$ and phase voltage vector $[V_{an},V_{bn},V_{cn}]^t$ is given in the equation (2)

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{Vdc}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2)$$

According to the equations (1) and (2) the eight possible combination of switching vectors, output line to neutral Voltage and output line – to – line voltages in terms of DC Link voltage V_{dc}, are given in Table I.

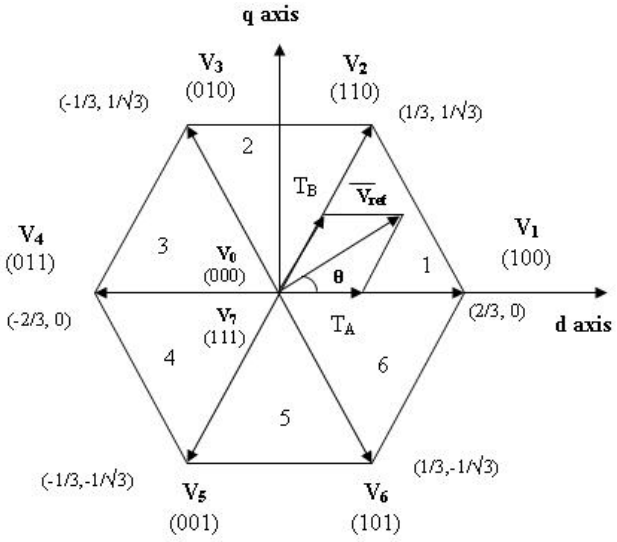

Fig.2.Basic Switching Vectors and Sectors

The switching time duration at any sector is can be calculated as follows:

$$T_A = T_C \cdot M\left[\sin\left(\frac{n}{3}\pi\right)\cos(\theta) - \cos\left(\frac{n}{3}\pi\right)\sin(\theta)\right]$$

$$T_B = T_C \cdot M\left[-\cos(\theta)\sin\left(\frac{n-1}{3}\pi\right) + \sin(\theta)\cos\left(\frac{n-1}{3}\pi\right)\right]$$

Where, n=1 to 6
$0° \le \theta \le 60°$
M- Modulation Index

$$T_0 = T_C - (T_A + T_B)$$

TABLE I
Switching Vector Table

Voltage vectors	Switching vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	Van	Vbn	Vcn	Vab	Vbc	Vca
V0	0	0	0	0	0	0	0	0	0
V1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V2	1	1	0	1/3	1/3	-2/3	0	1	-1
V3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V4	0	1	1	-2/3	1/3	1/3	-1	0	1
V5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V6	1	0	1	1/3	-2/3	1/3	1	-1	0
V7	1	1	1	0	0	0	0	0	0

3. FPGA Design Flow:

Xilinx system generator (XSG) is a plug-in tool developed for matlab/simulink package is used for Digital system modeling, algorithm development and verification purposes in digital signal processor (DSP), Field Programmable Gate Array (FPGA) Platforms. XSG acts as an interface by translating the simulink block sets model into VHDL code that can be embedded in FPGA chip. The first step in the development of a FPGA based controller begins with a mathematical model which describes the operation of the controller.

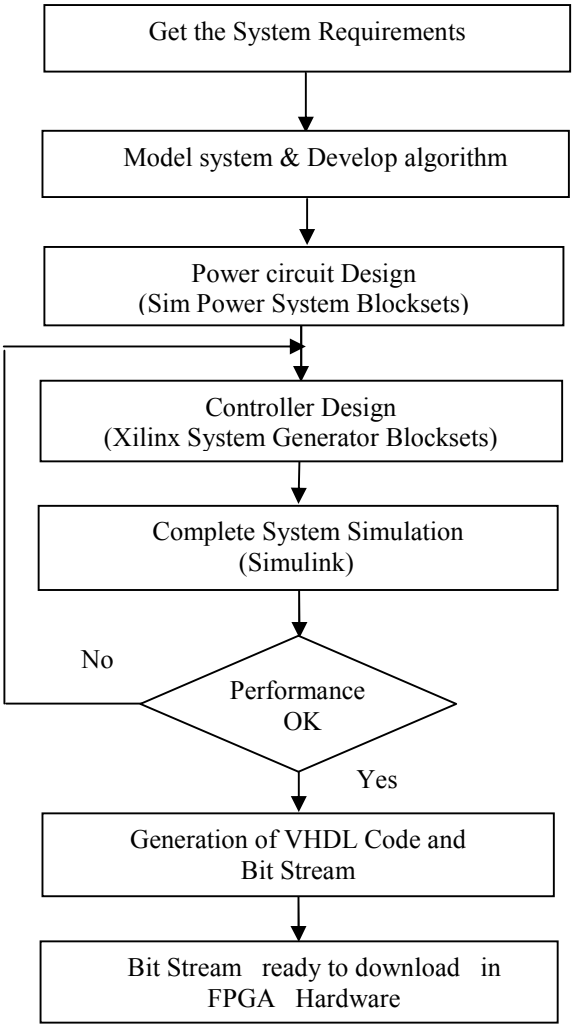

Fig.3.Design and Implementation process of FPGA Based Controller

The mathematical model was further developed as blocksets in XSG. Third step is to verify the simulated results manually. Fourth step is to generate VHDL code and bit stream from the XSG blocksets using XSG token. Finally the VHDL code and bit stream is embedded into FPGA chip [9-10].

4. Modeling of SVPWM - V/F Controller:

Initially an algorithm is designed and simulated at the system level with the floating point simulink blocksets. A Xilinx System Generator (XSG) is a plug-in tool to the Simulink modeling software which is used to derive hardware model of the system. The Xilinx block configuration that produced the model of SVPWM-V/F controller as presented in Fig(4).In this model the Gateway In1 and In2 is connected to the two switches in FPGA board which is used to incraese and decrease the set speed of the motor.

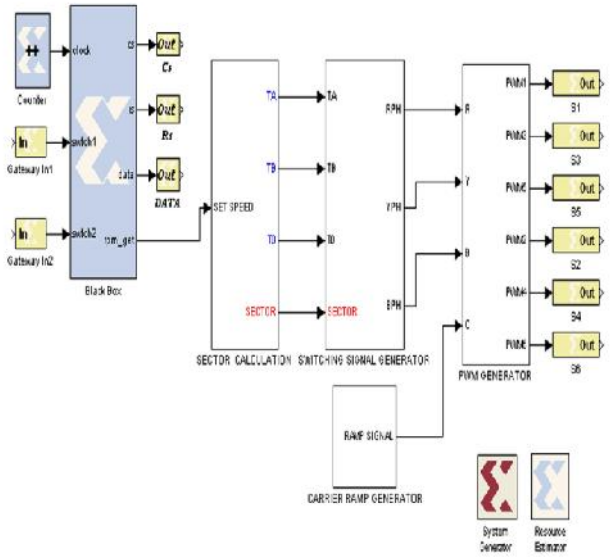

Fig.4.XSG Model of SVPWM-V/F Controller

The Xilinx black box is coded by VHDL coding to interface two switches and display the set speed into the LCD. The set speed is given to the sector calculation block, by using V/F control method the Amplitude, Teta and Sector value is calculated from the Set speed.

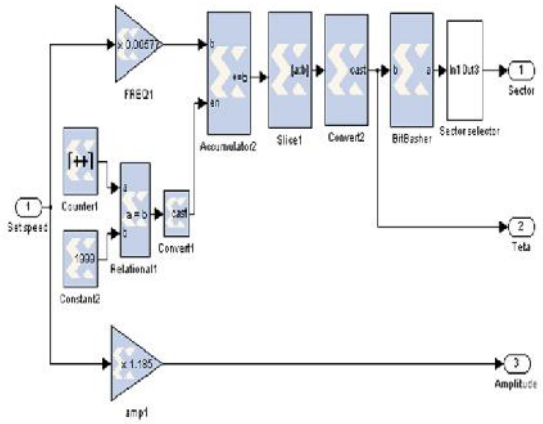

Fig.5.XSG Model of Sector Calculation

4.1.Design of Duty cycle calculator module:

The duty cycle time Ta,Tb,T0 is calculated from the amplitude and teta value as shown in this model.

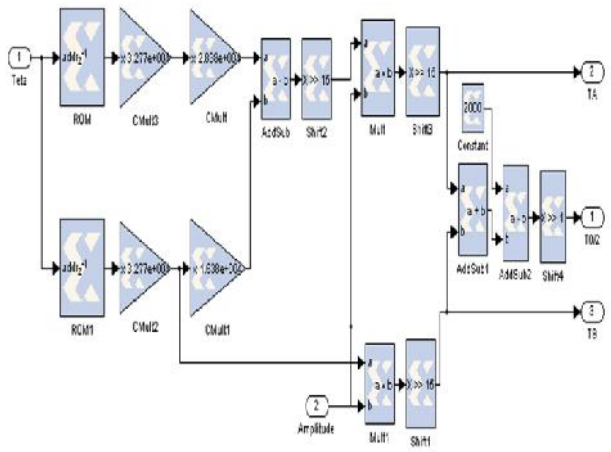

Fig.6.XSG Model of Duty Cycle Calculator

4.2. Design of Modulating signal generator module:

In this model the multiplexer is used to select the Duty cycle time of each phase based on the sector value and corresponding switching time is as shown in Fig.(7).Then finally it generates three phase modulating signal.

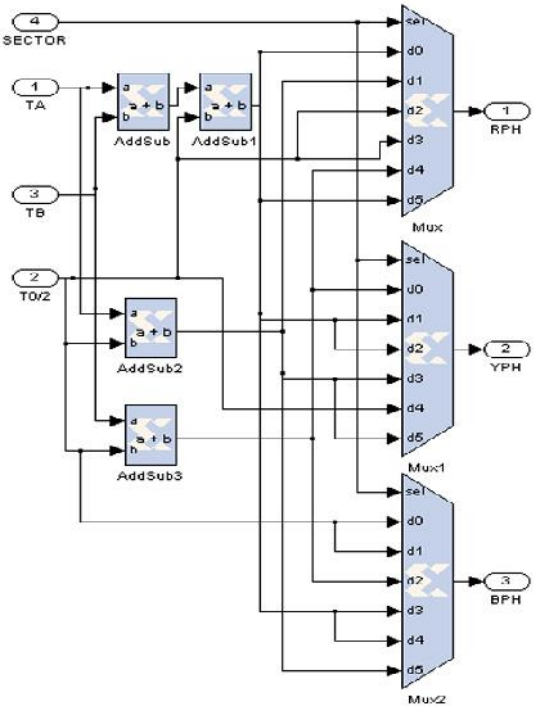

Fig.7.XSG Model of Modulating Signal Generator

4.3. Design of Carrier Ramp Signal Generator module:

The 10 KHz Carrier Ramp signal is generated by using 20 MHz system clock frequency as shown in this model. The Amplitude value of carrier signal is calculated as follows,

$$\text{Amplitude} = \frac{\text{FPGA System Clock frequency}}{\text{Carrier frequency}} = \frac{20MHZ}{10KHZ} = 2000$$

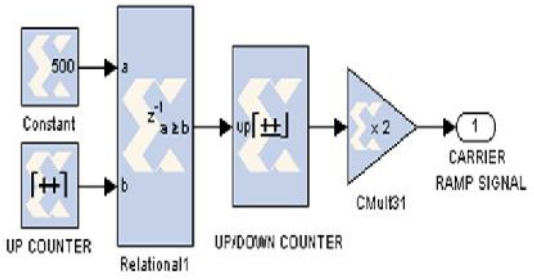

Fig.8. XSG Model of Carrier Ramp signal Generator

4.4. Design of SVPWM signal generator module:

In this model the Carrier Ramp signal is compared to three phase Modulating signal and generate the six type of space vector pwm pulses with dead time..

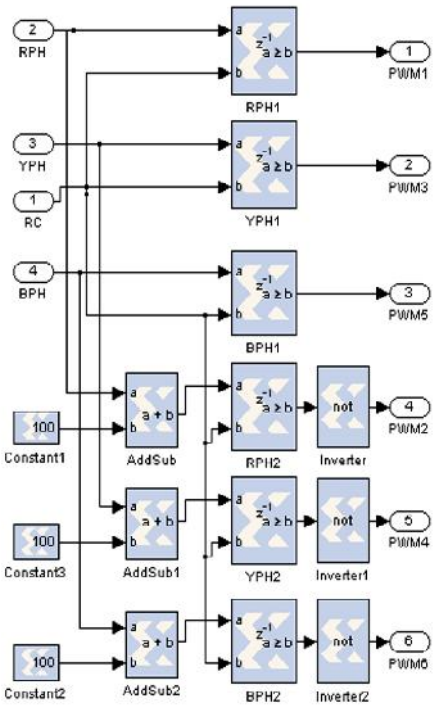

Fig.9.XSG Model of SVPWM signal Generator

5. FPGA SIMULATION RESULTS:

The SVPWM based V/F Controller for induction motor is simulated using Xilinx System Generator and Xilinx ISE Design suite 12.1.The switching patterns at various sectors of SVPWM are shown in Fig.10.(a-f).

It is inferred that the switching signal S_1, S_3, S_5 are given to the upper switches and S_2,S_4,S_6 are given to the lower switches of Three Phase Diode Clamped Two level Voltage Source Inverter to switch the input voltage of induction motor as shown in Fig.(1).

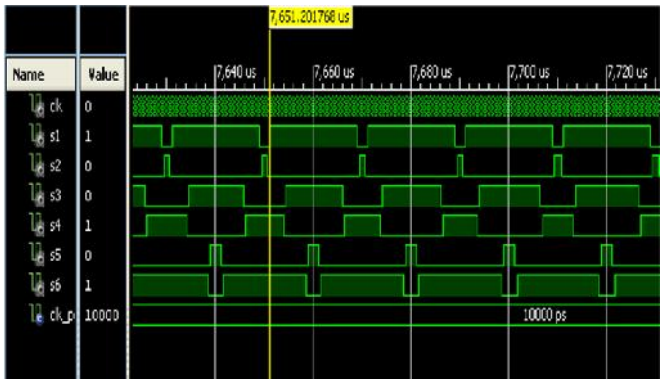

Fig.10 (a) XSG Simulation of SVPWM at Sector I

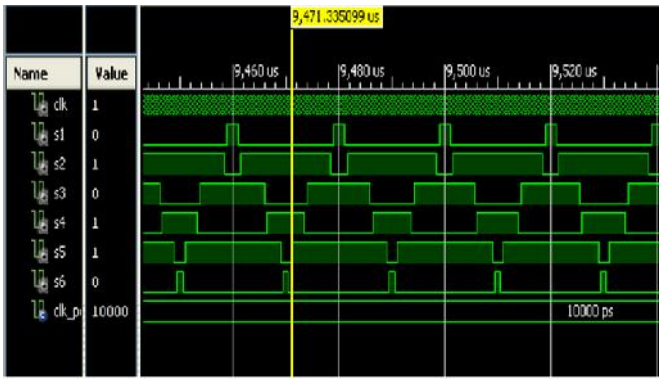

Fig.10 (d) XSG Simulation of SVPWM at Sector IV

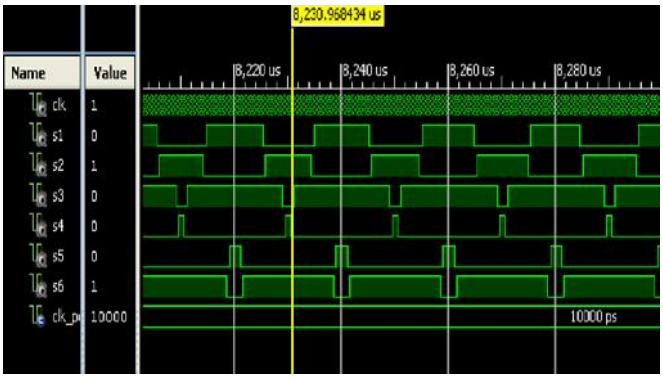

Fig.10 (b) XSG Simulation of SVPWM at Sector II

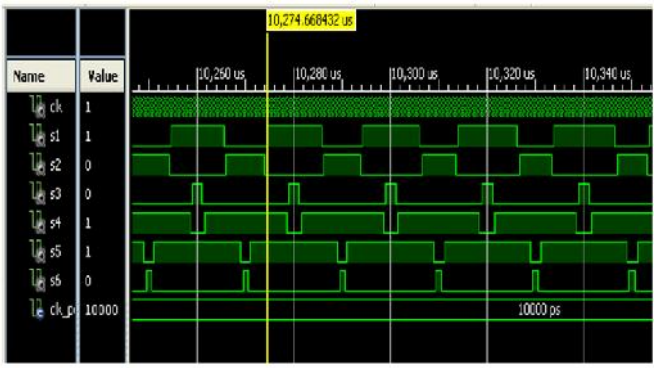

Fig.10 (e) XSG Simulation of SVPWM at Sector V

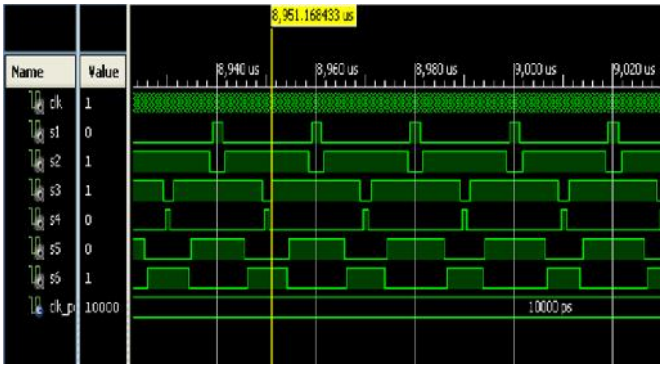

Fig.10(c) XSG Simulation of SVPWM at Sector III

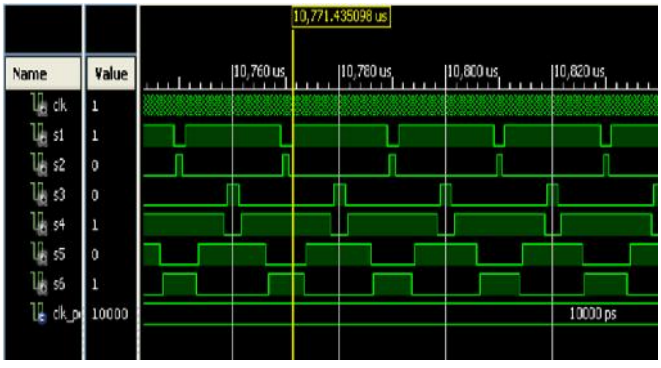

Fig.10 (f) XSG Simulation of SVPWM at Sector VI

5.1. Synthesis and Implementation Results:

The above designed model is synthesized using Xilinx Synthesis Tool (XST) and the Implementation process is done using Xilinx Plan Ahead Software. The results are presented in Table .The simulation of FPGA internal structure for designed controller is as shown in Fig. (11).

TABLE-II Design Summary

svpfinal_cw Project Status (04/05/2013 - 13:05:12)			
Project File:	svpfinal_cw.xise	**Parser Errors:**	No Errors
Module Name:	svpfinal_cw	**Implementation State:**	Placed and Routed
Target Device:	xc3s400-4pq208	**•Errors:**	No Errors
Product Version:	ISE 12.1	**•Warnings:**	523 Warnings (77 new)
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	All Constraints Met
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

TABLE-III FPGA Resource Usage

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	473	3584	13%
Number of Slice Flip Flops	251	7168	3%
Number of 4 input LUTs	871	7168	12%
Number of bonded IOBs	19	141	13%
Number of GCLKs	2	8	25%

Fig.11 Internal Structure of Designed controller in FPGA

6. EXPERIMENTAL RESULTS

In order to illustrate the efficiency of the proposed FPGA based Space vector modulated V/F Controller, Experiments were carried out on a Spartan3 - XC3S400 FPGA based prototyping platform as shown in Fig. (12).

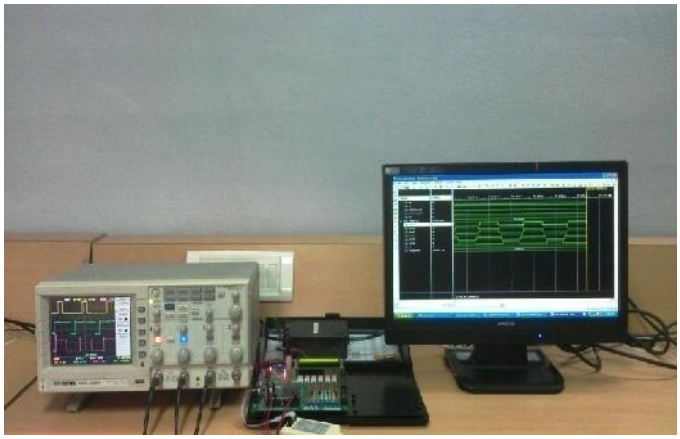

Fig.12.Experimental setup

Thus by implementing this controller in an FPGA, very good performance is reached. It's also processed with a different sampling frequency.

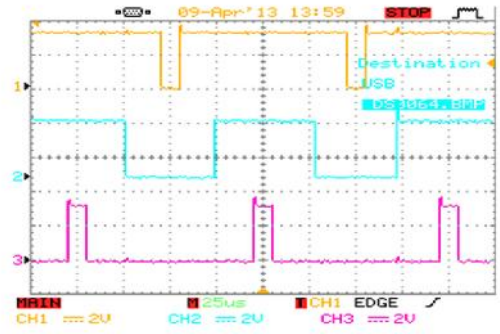

Fig.13 (a) SVPWM Signal at Sector 1

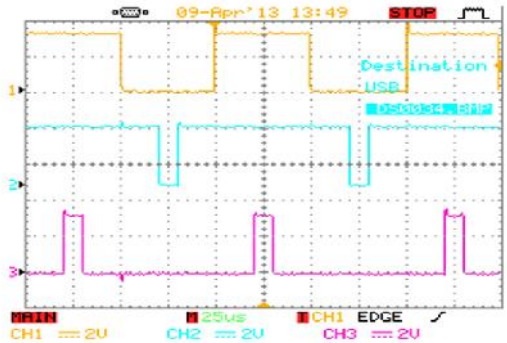

Fig.13 (b) SVPWM Signal at Sector 2

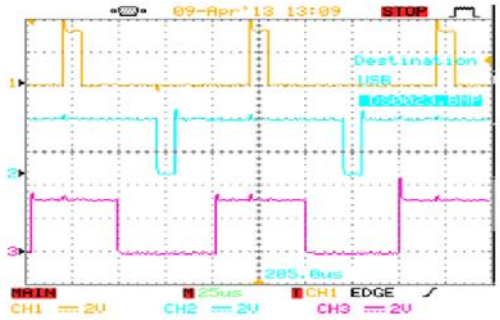

Fig.13(c) SVPWM Signal at Sector 3

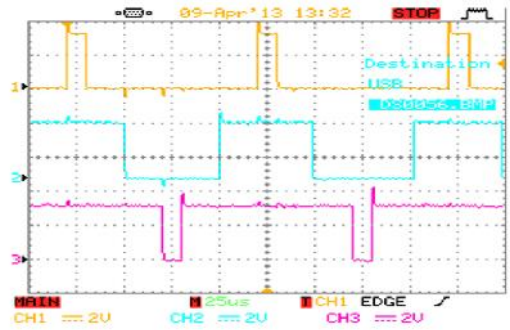

Fig.13 (d) SVPWM Signal at Sector 4

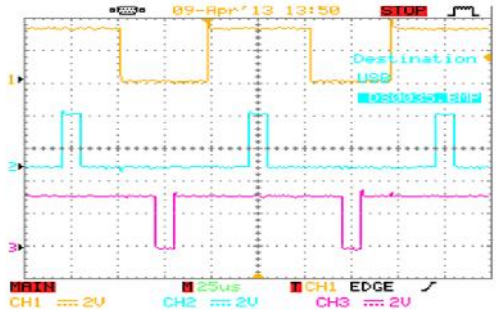

Fig.13 (e) SVPWM Signal at Sector 5

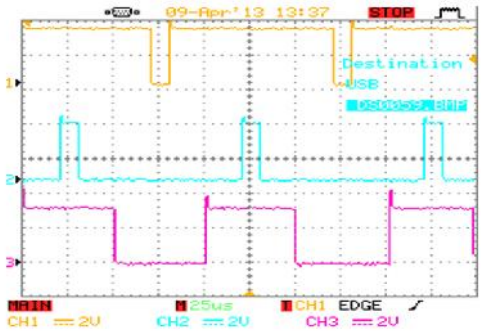

Fig.13 (f) SVPWM Signal at Sector6

The experimental results as shown in Fig.13(a-f) is SVPWM signal at different sectors with 10KHz Switching Frequency and Reference speed is 1350 , Modulation Index is 0.9.

7. CONCLUSION

The design and simulation of dynamically reconfigurable Control Structure for three phase induction motor drives was developed in this paper. The Important advantage of using Xilinx System Generator design structure is that it provides resource estimation details to the user, to select appropriate FPGA for his design .The high performance SVPWM-V/F Controller overcomes the drawbacks of Conventional Sinusoidal PWM Techniques Such as Variable Switching Frequency, Energy efficient, less harmonic distortions. The proposed concept is simulated and experimental results are presented. In future this system will be developed by using an Extended Kalman Filter and Direct Torque Control technique to design Sensorless Control system for Three phase Induction machine in FPGA Platform.

8. REFERENCES

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