Simulate and Analysis of the Limit of Output Capacitor Reduction in Power Factor Correctors by Distorting the Line Input Current

M.Sankar, G.Murugaraja, D.VasanthaKumar, S.Vignesh, B.Ramachendran

ABSTRACT*:* Active power-factor correctors (PFCs) are needed to implement ac–dc power supplies with input voltage and input current. The classical method to control PFCs consists in two feedback loops and an analog multiplier. Hence, the input current is ac and it is in-phase with the input voltage. However, a bulk capacitor is needed to balance the input and the output power. Due to its high capacitance, an electrolytic capacitor is traditionally used as a bulk capacitor in PFCs. As a consequence, the lifetime of the ac–dc power supply is mitigated by the electrolytic capacitors, which becomes insufficient to some applications (e.g., high brightness LEDs). This paper proposes a reduction of the output voltage ripple (which allows reduction of the output capacitance) by distorting the line input current, but maintaining the harmonic continent compatible with EN 61000-3-2 regulations. The limits of this output capacitor reductions are reduced. Also, a control strategy based on a low-cost pic microcontroller is developed to output the proposed study into practice. Finally, the theoretical results are validated in a 500-W prototype.

Index Terms— voltage ripple, harmonics, power factor correction.

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1.INTRODUCTION

In order to limit the harmonic content on the line current of mains-connected equipment, the use of an active power factor corrector (PFC) as a first stage of the two-stage solution is almost mandatory. Fig. 1(a) shows a general scheme of an active PFC controlled by two feedback loops, which is the most popular circuitry to control this type of power converters. In Fig. 1, the inner feedback loop is an input-current feedback loop and the outer one is an output-voltage feedback loop. The current loop makes the line current follow are reference signal, in phase with the input voltage, This is obtained by multiply in rectified sinusoidal waveform by v A(t). The output voltage of the voltage loop ($vA(t)$ is a dc voltage due to the low-pass filter placed in the voltage loop in order to obtain a sinusoidal line input current. Therefore, the pulsating input power is a square cosine function. In this case, a storage capacitor with large capacitance is required to balance the instantaneous power difference between the pulsating input power and the constant output power. A large capacitance is needed, and therefore, an electrolytic capacitor is often used as the storage capacitor. However, it is known that due to its liquid electrolyte, the lifetime of electrolytic capacitor is very limited. At this point, the output capacitor can be an obstacle to design an ac–dc power supply for long-lifetime loads, for example,ac–dc drivers for high-bright or long-lifetime power supplies, for example, no accessible or remote equipment[8]. Therefore, the power supply manufactures are looking for reducing this capacitance in order to avoid the use of an electronic capacitor. According to this idea, many of them offer lifetime warranty in the range of 5 to 10 years of lifetime [9].

1.1 Power Factor Correction Techniques

In recent years, single-phase switch-mode AC/DC power converters have been increasingly used in the industrial, commercial, residential, aerospace, and military environment due to advantages of high efficiency, smaller size and weight. However, the proliferation of the power converters draw pulsating input current from the utility line, this not only reduce the input power factor of the converters but also injects a significant amount of harmonic current into the utility line [9] To improve the power quality, various PFC schemes have been proposed. By the introduction of harmonic norms now power supply

manufacturers have to follow these norms strictly for the remedy of signal interference problem.

The various methods of power factor correction can be classified as:

(1) Passive power factor correction techniques

(2) Active power factor correction techniques

In passive power factor correction techniques, an LC filter is inserted between the AC mains line and the input port of the diode rectifier of AC/DC converter. This technique is simple and rugged but it has bulky size and heavy weight and the power factor cannot be very high. Therefore it is now not applicable for the current trends of harmonic norms. Basically it is applicable for power rating of lower than25W. For higher power rating it will be bulky. [7] in active power factor correction techniques approach, switched mode power supply (SMPS) technique issues' to shape the input current in phase with the input voltage. Thus, the power factor can reach up to unity. Figure 2 shows the circuit diagram of basic active power correction technique. By the introduction of regulation norms IEC 1000-3-2 active power factor correction technique is used now a day. There are different topologies for implementing active power factor correction techniques. Basically in this technique power factor correcting cell is used for tracking the input current in phase of input voltage such that input power factor come up to unity. Comparing with the passive PFC techniques, active PFC techniques have many advantages such as, high power factor, reduced harmonics, smaller size and light-weight. However, the complexity and relatively higher cost are the main drawbacks of this approach.

II. EXISISTING SYSTEM

In order to limit the harmonic content on the line current of mains-connected equipment, the use of an active power factor corrector (PFC) as a first stage of the two-stage solution is almost important. A general scheme of an active PFC controlled by two feedback loops, which is the most popular circuitry to control this type of power converters. The inner feedback loop is an input-current feedback loop and the outer one is an output-voltage feedback loop. The current loop makes the line current follow a reference signal, in phase with the input voltage, which is obtained by multiplying a rectified sinusoidal waveform (obtained from the line voltage) by vA(t). The output voltage of the voltage loop (vA(t)) is a dc voltage due to the low-pass filter placed in the voltage loop in order to obtain a sinusoidal line input current. Therefore, the pulsating input power is a square cosine function. In this case, a storage capacitor with large capacitance is required to balance the instantaneous power difference between the pulsating input power and the constant output power.

III. PROPOSED SYSTEM

The objective of this paper is to propose a method to reduce the storage capacitance, thus other capacitor technologies could be adopted instead of electrolytic capacitor to achieve long lifetime. Taking into account the energy transfer process of the PFC defined by its main waveforms, if the pulsating output current waveform (which is equal to the pulsating input power) was adequately modified, and then the amplitude of the output voltage ripple can be modified. [7]. The question is how the pulsating input power can be reduced. A possible solution consists on distorting the line input current.[10]Following this idea, the second section of this paper presents a study that analyzes the tradeoff between the line input current distortion and the output voltage ripple reduction in PFC.

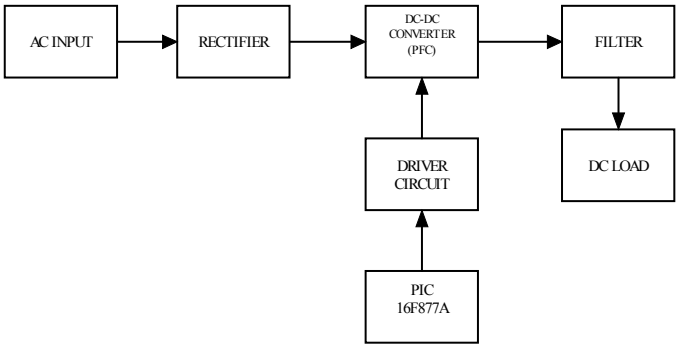

Fig 1: block diagram of power factor correctors

3.1 THE STATIC MODELING OF PFCS WITH FAST-OUTPUT-VOLTAGE FEEDBACK LOOP

The objective of this section is to determinate the evolution of the output voltage ripple when the line input current of the PFC is distorted. The static model of PFC with fast-output voltage feedback loop presented in useful for this study because it considers distortion in the line input current. This model describes the static behaviour of the PFCs when the bandwidth of the output-voltage feedback loop is increases.

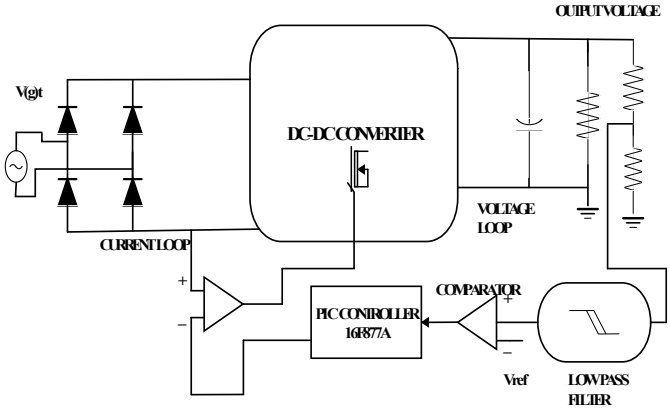

Fig 2 : circuit diagram of power factor correctors

$vg\ (\omega L\ t) = vgp\ |\sin(\omega L\ t)$

$ig(L\ t) = vgp\ |\sin(\omega L\ t)|\ vA(t)KM$

where $vgp$is the peak value of $vg\ (\omega L\ t)$, ωL is the line angular frequency, $vA(t)$ is the output voltage of the error amplifier, and KM is a constant

$VA(t) = vA\text{dc} + vA\text{ac}(t)$ (3)

$vA\text{ac}(t) = vA\text{ac}p\ \sin(2\omega L\ t)$

The pulsating output power [the power delivered by the power stage in can be obtained by multiplying the output voltage *vo*by the current *io* (*t*) injected by the power stage into the output cell made up of the bulk capacitor *CB* and the load *RL*

$Poi(\omega L\ t) = vo\ io\ (\omega L\ t)$.

The pulsating input power *pg* (*t*he value of the output voltage ripple can be calculated by multiplying the value of *io*2 ($\omega L\ t$) and *io*4 ($\omega L\ t$) by the impedance constituted by *CB* and *RL* connected in parallel. However, the impedance of *CB* at twice and at fourth, the line frequency must be much lower than *RL* in order to maintain the output voltage ripple in a reasonable value and, hence,

Solution	**PLC**	**ind-PC, VME**	**Micro controller/DSC**	**PIC controller**
Reliability	high	High	Medium	Medium
Flexibility	High	High	Medium	High
Advanced algorithms	Low	High	low/med	med/high
Costs	High	High	Low	med/low
Rapid prototyping	Low	High	low/high	low/high
Power Converter friendly	No	No	Yes	Yes

the parallel impedance of *CB* and *RL* can be approximated by the impedance of *CB*

$.Vo(t) = vo + vo\text{ac}(t) = vo + 2vo2\omega l(2 + k\sin\varphi L) \times -k$ $\cos(2\omega L\ t - \varphi L) - \sin(2\omega L\ t)$

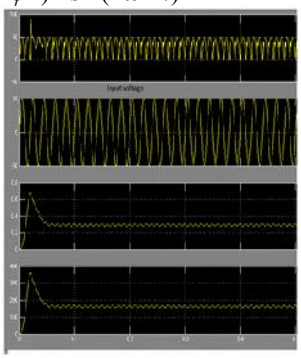

Fig 3 : Simulation output waveform

Fig 4: Hardware kit for power factor correctors

IV. PIC CONTROLLER

PIC controllers are still predominantly used in the industry for most of the motion control applications, because of their simplicity, real-time control capability, easy implementation, and cost effectiveness. Ref[15/]PIC controllers, however, may not work properly if system parameters change or outer disturbances are present. In addition, PIC controllers for nonlinear systems do not work

The power factor calculation is achieved by Simulink/ Mat lab simulation using the appropriate models for the system which is shown in figure 1. First, the simulation has been carried out without input passive filter for two different loads: a) ohmic load and b) ohmic inductive load (several values), by a switching frequency fsw=5 kHz. The power factor as a function of the angle ‘a ‘mentioned above is depicted in the figures 4, 5 for an effective load power of P=1200W. Figure 14 shows the power factor in the case that a DC motor is used as a load. In figure 15 is PF=f(‘a’) by fsw=10 kHz. In figures11 and 12 the waveforms of the ac input voltage and current are shown. The figures 6, 7, 8, 9 and 10 show the spectrum of the input current for characteristic values of the angle ‘a’. In the case of ohmic load (R=20Ω) the power factor gets its maximum value (PFmax=0,6548) by ‘a’=0°, which is relatively a low value because of the great current high harmonic content. If the load has ohmic inductive character, the maximum PF value is obtained by a negative value of angle ‘a’. This happens because the control voltage Uc mentioned above is leading by the angle ‘a’ upon the grid voltageVg ,in order to achieve that the basic current harmonic is in phase with the grid voltage. In this point it must be remarked that the PWM procedure, controlled by the signal Uc, leads to the correction of the power factor through the moving of the current waveform to the left in the figure 12, what can be easy shown if the figures 11 and 12. So, the waveforms of uin(t) and iin(t) get more similar to the waveform of figures 13. But, by moving of the wave form iin(t) increase the high harmonic content, as it can be shown in the figures 6, 7, 8, 9 and 10, which are getting through FFT analysis of the input current waveform iin(t) using the Origin software. It is obviously that the high harmonic content of I in(t), for example, by ‘a’=0° is lower than that by ‘a’=-45o (fig.7 and 10). Beginning from ‘a’=0° and gradually going on to ‘a’=-45° the harmonics of the 5th, 7th, 9th and 11th order increase

3.2: Table microcontroller versus PIC controller

as expected due to the fact that fixed controller gains have lack of flexibility to deal with nonlinear effects.

For the remedy of this defect of PIC controllers, many control algorithms have been presented. The adaptive control method has been used to tune PIC controller gains against system parameter variations. The robust control method has been used to reject disturbances. Advanced control theories have been well developed to tackle system uncertainties, and although they may solve problems associated with the PIC controller, they require system dynamic models to derive the adaptive control laws and the robust control laws. An added challenge is that the required system dynamic models are often unavailable or hard to obtain. The pin diagram of Peripheral Interface Controller (PIC) is as shown in the figure 1.13. This device is electrically erasable, and can therefore be offered in a low cost plastic package. Being electrically erasable, these devices can be both erased and reprogrammed without removal from the circuit. An EEPROM device allows its memory to be erased by an electric charge. PIC is used to generate Pulse Width Modulation (PWM) wave by comparing sine wave and oscillatory wave. It consists of totally 40 pins of which 33 pins are divided into five ports .Remaining pins are multiplexed with an alternate function for the peripheral features on the device. General purpose I/O pins can be considered the simplest of peripherals. They allow the PIC microcontroller to monitor and control other devices.

4.1 Bridge Rectifier Circuit

The Circuit diagram of bridge rectifier is a Step-down transformer is used to step down the input AC voltage to 12V.Rectifier circuit consists of inductors, capacitors, diodes and voltage regulator. Here the 12V AC is converted into 12V DC .The voltage regulator LM 7805 convert 12V DC supply to 5V DC supply and regulates it.

4.2 PORTA and the TRISA Resistor

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read; the value is modified and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open-drain output. All other PORTA pins have TTL input levels and full CMOS output drivers. Other PORTA pins are multiplexed with analog inputs and the analog VREF input for both the A/D converters and the comparators. The operation of each pin is selected by clearing/setting the appropriate control bits in the ADCON1 and/or CMCON registers. The TRISA register controls the direction of the port pins even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

4.3 PORTB and the TRISB Register

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

In-Circuit Debugger and Low-Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in "Special Features of the CPU". Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB. This will end the mismatch

b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared. The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

This interrupt-on-mismatch feature, together with software configurable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression.

4.4 PORTC and the TRISC Register

PORTC is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin). PORTC is multiplexed with several peripheral functions (Table 4-5). PORTC pins have Schmitt Trigger input buffers. When the I2C module is enabled, the PORTC<4:3> pins can be configured with normal I2C levels, or with SM Bus levels, by using the CKE bit (SSPSTAT<6>).When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the

TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify write instructions (BSF, BCF, and XORWF) with TRISC as the destination, should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

4.5 PORTD and TRISD Registers

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output. PORTD can be configured as an 8-bit wide microprocessor port (Parallel Slave Port) by setting control bit, PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

V. CONCLUSION

In summary, this paper proposes a method to reduce the storage capacitance in PFCs. The results show that reductions of 50% in Class A and B, 23% in Class C, 38% in Class D, and 34% in Energy Star program requirements for SSL luminaries can be achieved. Taking into account these output capacitor reductions, it is difficult to remove the electrolytic capacitor only by distorting the line input current. A possible solution is to distort the input current and to allow a significant ripple in the output voltage in order to remove the electrolytic capacitor. In this case, a second stage is needed in order to eliminate the low-frequency ripple.

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