Design Incrementing Burst Data Transfer Operation for AMBA-Advanced High Performance Bus

Mital Mungra and Assi. Prof. Vishal S.Vora

Abstract: The rapid development in the field of mobile communication, digital signal processing motivated the design engineer to integrate the complex systems of multimillion transistors in a single chip. The design of an AMBA advanced high performance bus (AHB) protocol basic block is presented. Operations like simple read write and burst read write and out of order read write are mentioned. The AHB (Advanced High-performance Bus) is a high-performance bus in AMBA (Advanced Microcontroller Bus Architecture) family. This AHB can be used in high clock frequency system modules. The design of the AHB Protocol is simulated using Modelsim which has the basic blocks such as Master and Slave. The arbitration mechanism is used to ensure that only one Master has access to the bus at any one time and the AHB decoder is used to decode the address of each transfer and provide a select signal for the slave that is involved in the transfer .It can be coded using VHDL.

Keywords: AHB bus matrix, arbiter, system on chip, FSM for master and slave, master and slave side arbitration, IP, VHDL..

I. INTRODUCTION

In recent days, the development of SOC chips and the reusable IP cores are given higher priority because of its less cost and reduction in Time to market. So this enables the major and very sensitive issue such as interfacing of these IP cores. These interfaces play a vital role in SOC and should be taken care because of the communication between the IP cores properly. The communication between the different IP cores should have a lossless data flow and should be flexible to the any SOC designer too. Hence to resolve this issue, the standard protocol buses are used in or order to interface the two IP cores. There are many bus interfaces are available in the market. Most of the IP cores from ARM use the AMBA (Advanced Microcontroller Bus Architecture) which has AHB (Advanced High-Performance Bus).

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The purpose of this work is to implement different operation of data transfer for a SOC bus for Open Cores that we would adopt and use in any core development. There exist many bus interfaces AMBA, CORECONNECT, WISHBONE, AVALON are well known and well used bus architectures. AMBA offers advantage compared to all other buses.It can be coded using any hardware description language like VHDL and VERILOG, and it takes the shapes of simple logic gates supported by most of FPGAs and ASIC devices.

AMBA bus which can support up to 16 Master and 16 Slave .The benefits of the SOC approaches are numerous, including improvements in system performance, cost, size and power dissipation. This bus has its own advantages and flexibilities. A full AHB interface is used for the following.

- Bus Masters
- On-chip memory blocks
- External memory interfaces
- High-bandwidth peripherals with FIFO interfaces
- DMA slave peripherals

II. AMBA-AHB PROTOCOL

A. Objective of the AMBA-AHB

1. It gives Facility to right-first-time development of embedded microcontroller products with one or more CPUs, GPUs or signal processors.
2. It is technology independent, to allow reuse of IP cores, peripheral and system macro cells across diverse IC processes
3. It encourages modular system design to improve processor independence, and the development of reusable peripheral and system IP libraries.
4. It minimize silicon infrastructure while supporting high performance and low power on-chip communication.

B. A Typical AMBA based architecture

The Figure I shows the typical AMBA based Microcontroller system. The Advanced Microprocessor Bus

Architecture (AMBA) defined by ARM is a widely used open standard for an on-chip bus system. An AMBA-based microcontroller typically consists of a high-performance system backbone bus (AMBA AHB or AMBA ASB), able to sustain the external memory bandwidth, on which the CPU, on-chip memory and other Direct Memory Access (DMA) devices reside. In older version it used ASB as a backbone bus or in new version it used AHB as backbone bus. This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers. The system busses ASB and AHB are designed for high performance connection of processors, dedicated hardware and on chip memory. They allow following things :

1. Multiple bus Masters
2. Pipelined operation
3. Burst transfers
4. Split transactions
5. High performance

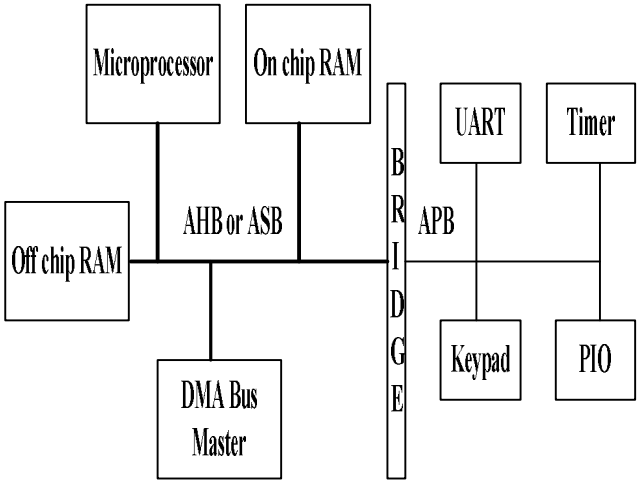


Figure I : A typical AMBA based architecture

The main aim of this to make ease the component design ,by allowing the combination of interchangeable components in the SOC design. It promotes the reuse of intellectual property components, so that at least a part of the SOC design can become a composition, rather than a complete rewrite every time. By referring The Advanced Microcontroller Bus Architecture (AMBA) specification 2.0, it defines an on chip communications standard for designing high-performance embedded microcontrollers. Three distinct buses are defined within the AMBA specification:

1. The Advanced High-performance Bus (AHB)
2. The Advanced System Bus (ASB)
3. The Advanced Peripheral Bus (APB)

1. Advanced High-performance Bus (AHB)

The AMBA AHB is for high-performance, high clock frequency system modules. The AHB acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macro cell functions. AHB is also specified to ensure ease of use in an efficient design flow using synthesis and automated test techniques.

2. Advanced System Bus (ASB)

The AMBA ASB is for high-performance system modules. AMBA ASB is an alternative system bus suitable for use where the high-performance features of AHB are not required. ASB also supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macro cell functions.

3. Advanced Peripheral Bus (APB)

The AMBA APB is for low-power peripherals. AMBA APB is optimized for minimal power consumption and reduced interface complexity to support peripheral functions. APB can be used in conjunction with either version of the system bus.

C. Choice of system bus

Both AMBA AHB and ASB are available for use as the main system bus. Typically the choice of system bus will depend on the interface provided by the system modules required. The AHB is recommended for all new designs, not only because it provides a higher bandwidth solution, but also because the single-clock-edge protocol results in a smoother integration with design automation tools used during a typical ASIC Development. It also have features that is not available with ASB

A full AHB or ASB interface is used whenever we want to implement or need to connect the components described below.

- Bus Masters
- On-chip memory blocks
- External memory interfaces
- High-bandwidth peripherals with FIFO interfaces
- DMA slave peripherals.

A simple APB interface is used whenever we want to implement or need to connect the components described below.

- Simple register-mapped slave devices
- Very low power interfaces where clocks cannot be globally routed

- Grouping narrow-bus peripherals to avoid loading the system bus.

D. Terminology

The following terms are used throughout this specification:

1. Bus Cycle:

A bus cycle is a basic unit of one bus clock period and for the purpose of AMBA AHB or APB protocol descriptions is defined from rising-edge to rising-edge transitions. An ASB bus cycle is defined from falling-edge to falling-edge transitions. Bus signal timing is referenced to the bus cycle clock.

2. Bus Transfer:

An AMBA AHB bus transfer is a read or write operation of a data object, which may take one or more bus cycles. The bus transfer is terminated by a completion response from the addressed slave. The transfer sizes supported by AMBA AHB include byte (8-bit), half word (16-bit) and word (32-bit).

3. Burst Operation :

A burst operation is defined as one or more data transactions, initiated by a bus master, which have a consistent width of transaction to an incremental region of address space. The increment step per transaction is determined by the width of transfer (byte, half word and word).

E. Features

- High performance
- Burst transfers
- Split transactions
- Single edge clock operation
- SEQ, NONSEQ, BUSY, and IDLE Transfer Types
- Programmable number of idle cycles
- Large Data bus-widths - 32, 64, 128 and 256 bits wide
- Address Decoding with Configurable Memory Map

III. MERITS AND DEMERITS

A. Merits ;

- AHB offers a fairly low cost (in area), low power (based on I/O) bus with a moderate amount of complexity and it can achieve higher frequencies when compared to others because this protocol separates the address and data phases.
- AHB can use the higher frequency along with separate data buses that can be defined to 128-bit and above to achieve the bandwidth required for high-performance bus applications.
- AHB can access other protocols through the proper bridging converter. Hence it supports the bridge configuration for data transfer.
- AHB allows slaves with significant latency to respond to read with an HRESP of “SPLIT”. The slave will then request the bus on behalf of the master when the read data is available. This enables better bus utilization.
- AHB offers burst capability by defining incrementing bursts of specified length and it supports both incrementing and wrapping. Although AHB requires that an address phase be provided for each beat of data, the slave can still use the burst information to make the proper request on the other side. This helps to mask the latency of the slave.
- AHB is defined with a choice of several bus widths, from 8-bit to 1024-bit. The most common implementation has been 32-bit, but higher bandwidth requirements may be satisfied by using 64 or 128-bit buses.
- AHB used the HRESP signals driven by the slaves to indicate when an error has occurred.
- AHB also offers a large selection of verification IP from several different suppliers. The solutions offered support several different languages and run in a choice of environments.
- Access to the target device is controlled through a MUX, thereby admitting bus-access to one bus-master at a time.
- AHB Masters, Slaves and Arbiters support Early Burst Termination. Bursts can be early terminated either as a result of the Arbiter removing the HGRANT to a master part way through a burst or after a slave returns a non-OKAY response to any beat of a burst. However that a master cannot decide to terminate a defined length burst unless prompted to do so by the Arbiter or Slave responses.
- Any slave which does not use SPLIT responses can be connected directly to an AHB master. If the slave does use SPLIT responses then a simplified version of the arbiter is also required.

B. Demerits :

- AHB cannot achieve full data bus utilization and bandwidth if some slaves have a relatively high latency.
- AHB defines transfer sizes of 1, 2, 4, 8, and 16 bytes. Because byte enables are not defined, there are cases where multiple transfers must be made inside a single quadword.
- AHB defines timing parameters for many of the relationships between signals on the bus. However, these are not associated with requirements relative to a clock cycle. Therefore,
  SoC developers must integrate AHB cores and run chip level static timing analysis to judge how compatible AHB masters and slaves are with one another.
- Power-based SoCs cover a wide range of applications, and there is a corresponding wide range of address map requirements. Having the address decodes for all AHB slaves reside within the interconnect means having to support the most complex split address ranges, even for the simplest of slaves

IV. BLOCK DIAGRAM OF AMBA_AHB

A. Component of the block diagram :

Totally this block diagram comprises of four components.

- Arbiter
- Master
- Slave
- Decoder

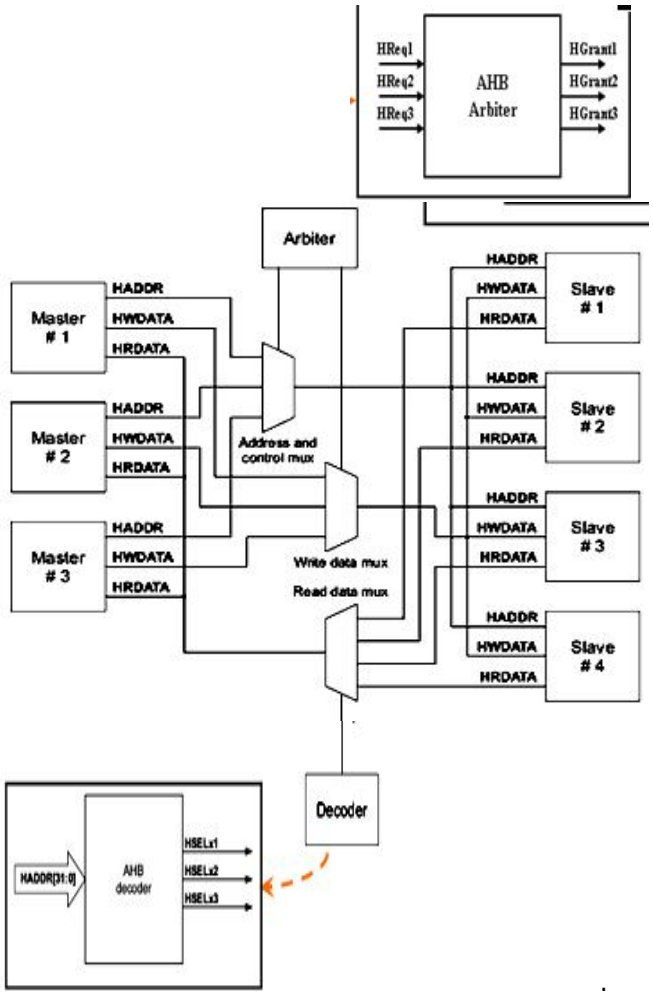


Figure II : block diagram of AMBA-AHB

1. Arbiter :

The arbitration mechanism is used to ensure that only one master has access to the bus at any one time. The arbiter performs this function by observing a number of different requests to use the bus and deciding which is currently the highest priority master requesting the bus.

2. Master :

A bus master is able to initiate read and write information by providing address and control information. Only one bus master can use the bus at the same time An AHB bus master has the most complex bus interface in an AMBA system. Typically an AMBA system designer would use predesigned bus masters and therefore would not need to be concerned with the detail of the bus master interface. No provision is made within the AHB specification for a bus master to cancel a transfer once it has commenced.

3. Slave :

After a master has started a transfer, the slave then determines how the transfer should Progress the transfer should progress. Whenever a slave is accessed it must provide a response which indicates the status of the transfer. The HREADY signal is used to extend the transfer and this works in combination with the response signal HRESP which provide the status of the transfer. The slave can complete the transfer in a number of ways. It can:

- Complete the transfer immediately
- Signal an error to indicate that the transfer has failed
- Delay the completion of the transfer, but allow the master and slave to back off the bus, leaving it available for other transfers.

4. Decoder :

The AHB decoder is used to decode the address of each transfer and provide a select signal for the slave that is involved in the transfer. A central address decoder is used to provide a select signal 'HSELx' for each slave on the bus. The select signal is a combinatorial decode of the high-order address signals. A slave must only sample the address and control signals and HSELx is asserted when HREADY is HIGH, indicating that the current transfer is completing.

B. Working :

The AMBA AHB bus protocol is designed with a central multiplexor interconnection scheme. Using this scheme all bus masters drive out the address and control signals indicating the transfer, they wish to perform and the arbiter determines which master has its address and control signals routed to all of the slaves.

Before which initially the master who needs to perform the operation should give the request signal to the arbiter and the arbiter will give the grant signal to the master for further proceedings. Similarly, a decoder is used to select the slave which has to be active during the operation based on the address given by the master.

A central decoder is also required to control the read data and response signal multiplexor, which selects the appropriate signals from the slave that is involved in the transfer. These make the read and write operation smoothly.

C. AMBA-AHB Signal :

All signals are prefixed with the letter H, ensuring that the AHB signals are differentiated from other similarly named signals in a system design. The signals involved in designing the AMBA AHB are listed in the Table I which also gives the specification of each signal.

Table I : AHB signal list

S.No.	NAME	WIDTH	DRIVER	FUNCTION
1	HCLK	1	Clock Source	This clock times all bus transfers at the rising edge of HCLK
2	HADDR	32	Master	The system address bus of width 32-bit
3	HTRANS	2	Master	Indicates the type of the current transfer happening
4	HWRITE	1	Master	When HIGH this signal indicates a write transfer and when LOW a read transfer
5	HSIZE	3	Master	Indicates the size of the transfer
6	HBURST	3	Master	Indicates if the transfer forms part of a burst.
7	HWDATA	8	Master	The write data bus is used to transfer data from the master to the bus slaves during write operations.
8	HSELx	1	Decoder	Each AHB slave has its own slave select signal and this signal indicates that the current transfer is intended for the selected slave.
9	HRDATA	8	Slave	The read data bus is used to transfer data from bus slaves to the bus master during read operations.
10	HREADY	1	Slave	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer.
11	HRESP	2	Slave	The transfer response provides additional information on the status of a transfer

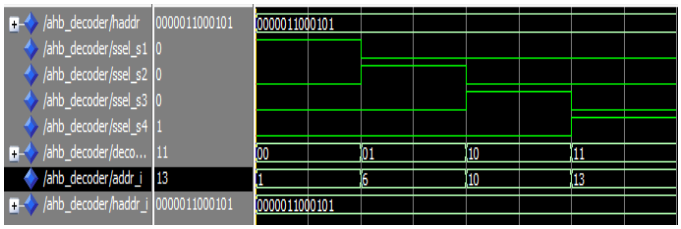
V. APPLICATIONS

AMBA-AHB can be used in the different application and also it is technology independent.

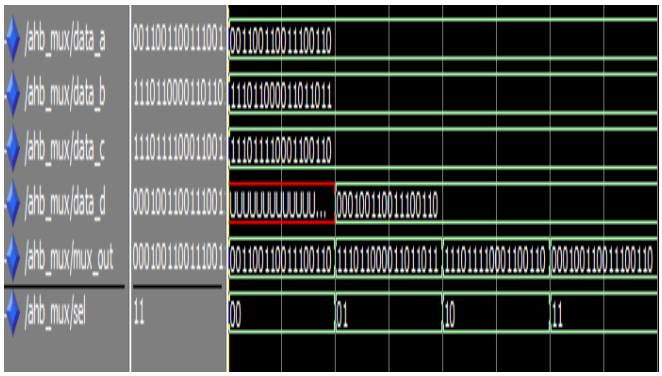
- ARM Controllers are designed according to the specifications of AMBA.
- In the present technology, high performance and speed are required which are convincingly met by AMBA-AHB
- Compared to the other architectures AMBA-AHB is far more advanced and efficient.
- To minimize the silicon infrastructure to support on-chip and off-chip communications.
- Any embedded project which involve in ARM processors or Microcontroller must always make use of this AMBA-AHB as the common bus throughout the project.

VI. RESULTS

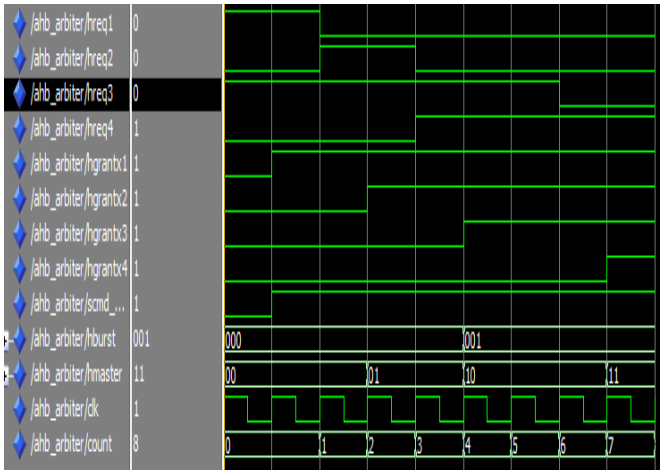
A. Simulation result of Decoder :



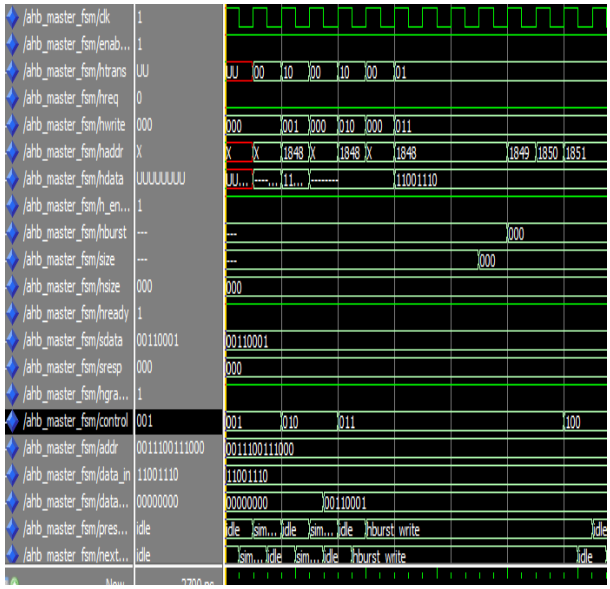
B. Simulation result of Multiplexer :

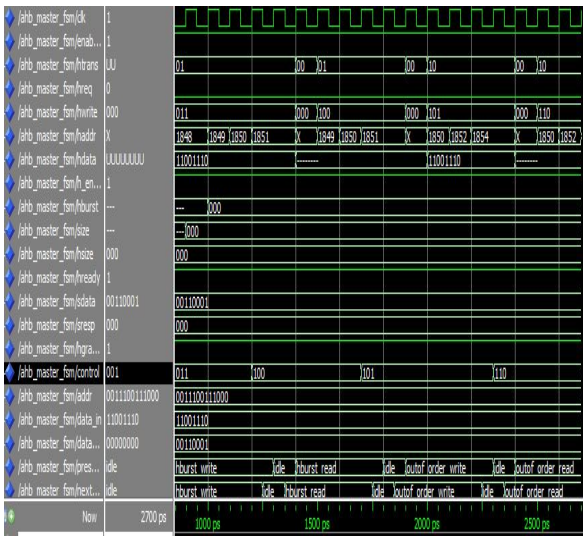


C. Simulation result of Highest priority algoritham :

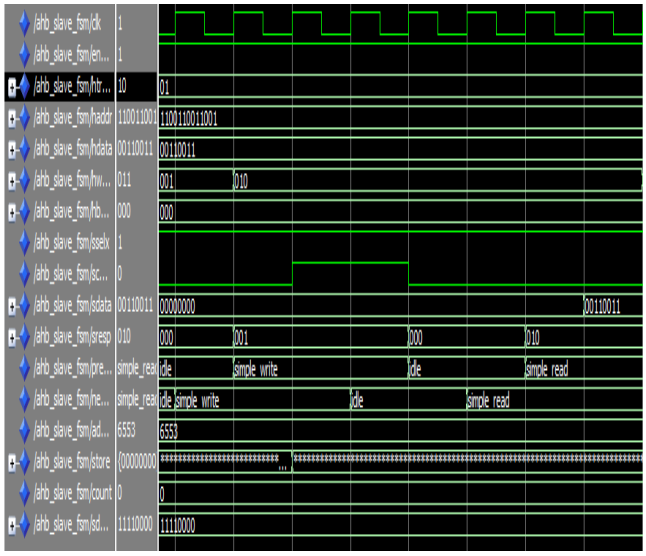


D. Simulation result of Master :





E. Simulation result of Slave :



VII. CONCLUSION

The AMBA advanced Microcontroller bus architecture specification defines an On-Chip Communications standard for designing high performance embedded microcontrollers. I have designed the intellectual properties of the Master and Slave depending upon the specifications, data transfer and various transfer modes that are supported by AMBA-AHB architecture. All of the commands and data are successfully transferred from one IP core to the other IP core using AMBA-AHB protocol. There is no loss of data or control information. The main goal of this work is to design algorithms for arbiter which is useful to granting the Master. The design of decoder is also completed which is generating the select signal for the slave. Also different operation of data transfer is also mentioned

APPENDIX

AMBA – Advanced Microcontroller Based Architecture.
AHB – Advanced High performance Bus.
ASB – Advanced System Bus.
APB – Advanced Peripheral Bus.
SOC – System On Chip.
IP – Intellectual Property
VHDL – Very high speed integrated circuit Hardware Descriptive Language.

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