# Parallel Power Flow AC/DC Converter with Input Power Factor Correction and Tight Output Voltage Regulation for Universal Voltage Applications

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**Abstract: A new parallel-connected power flow topology is proposed to improve the input power factor with simultaneously output voltage regulation taking consideration of current harmonic norms. Paralleling of converter modules is a well-known technique that is often used in medium-power applications to achieve the desired output power by using smaller size of high frequency transformers and inductors. The proposed approach offers cost effective, compact and efficient AC-DC converter by the use of parallel power processing. One converter primarily regulates output voltage with fast dynamic response and it acts as master which processes 60% of the power. Other converter with AC/DC PFC stage regulates input current shaping and PFC, and processes the remaining 40% of the power as a slave. This paper presents a design example and circuit analysis for 200 W power supply. Along with this a fly back converter is also simulated to show merits and comparison of performance. A parallel-connected interleaved structure offers smaller passive components, high efficiency, and reduced volt-ampere rating of DC/DC stage converter. MATLAB/SIMULINK is used for implementation and simulation results show the performance improvement.**

Key words: Parallel power flow, Power Factor Correction, Power quality.

### 1.1 Background

Most electronic equipment is supplied by 50-60 Hz utility power, and more than 50% of this power is processed through some kind of power converter. Usually power converters use a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage. Since these power converters absorb energy from the AC line only when the line voltage is higher than the DC bus voltage, the input line current contains rich harmonics, which pollute the power system and interfere with other electric equipment. These converters usually have a low power factor of 0.65. More stringent international requirements to limit the line input current harmonics, such as IEC 1000, have been effected recently. Because the conventional simple diode rectifier followed by a bulk capacitor cannot meet the requirements, which have stimulated the research of power factor correction techniques.

**Power Factor (*PF*):** The power factor is defined as the ratio of the average power to the apparent power at an AC terminal.

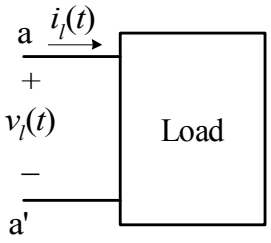


**Fig 1.1 Electrical utility**

$$PowerFactor\,(PF) = \frac{Real\ Power(Average)}{Apparent\ Power}$$

Figure 1.1 shows the electrical utility system in which the supply is given to load. Depending upon the type of load the power factor is defined for two types:

(i) Linear Load
(ii) Non-Linear Load

**Linear Load:** Assuming an ideal sinusoidal input voltage source, when the load is linear the current drawn by the load is also sinusoidal in nature as shown in Figure 1.2. So, the power factor can be expressed cosine of the angle between the voltage and current.

$$PF = \frac{I_{rms} V_{rms} \cos\theta}{I_{rms} V_{rms}} = \cos\theta$$

**Non-Linear Load:** The power factor for a non-linear load is defined as the product of two factors, the distortion factor and the displacement factor, as given in Eq. (1.1) and Figure 1.2 shows the input current and voltage waveform for a non-linear load. The distortion factor $K_d$ is the ratio of the fundamental root-mean-square (RMS) current to the total RMS current. The displacement factor $k_\theta$ is the cosine of the displacement angle between the fundamental input current and the input voltage.

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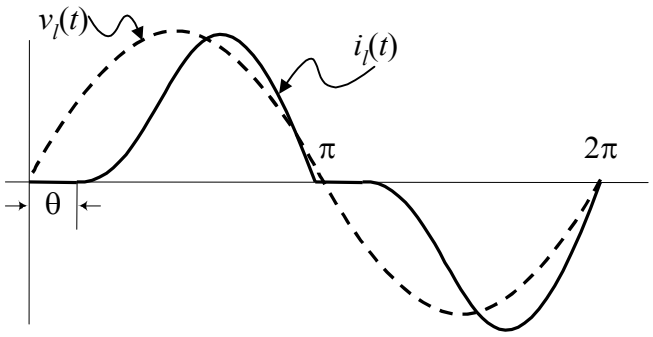



Fig 1.2 Input Voltage and Current for Non-Linear Load

$$PF = \frac{}{V_{rms} I_{rms}}$$
$$= \frac{I_{rms(1)}}{I_{rms}} \cos\theta \qquad (1.1)$$
$$= K_d K_\theta$$

When a converter has less than unity power factor, it means that the converter absorbs apparent power higher than the real power it consumes. This implies that the power source should be rated with higher VA ratings than the load needs. In addition, the current harmonics the converter produces deteriorate the power source quality, which eventually affect the other equipment. The simple solution to improve the power factor is to add a passive filter, which is usually composed of a capacitor and an inductor. However, this passive filter is bulky and inefficient since it operates at the line frequency. Therefore, a power factor correction stage has to be inserted to the existing equipment to achieve a good power factor. Usually, two types of power factor correction methods are used: the VAR/harmonics compensation method and the off-line PFC method [1-4]. The VAR/harmonics compensation method employs a switch-mode power converter in parallel with the nonlinear load to supply a reactive power and/or line current harmonics to cancel the displacement and the line current harmonics created by the nonlinear load. This method cannot cancel all the line current harmonics, however, and this additional line current harmonics compensator cannot regulate the output to the load. The high frequency switch mode power factor correction converter [1-4], called a PFC stage, is usually inserted in the equipment to shape the line input current into a sinusoidal waveform and its line current is in phase with the line voltage.

This project will focus on the development of the advanced power factor correction techniques.

Project is organized in abstract, eight chapters and references. Chapter-I includes introduction and requirement of work. Chapter-II discusses different techniques of PFC with advantages and disadvantages. Discussion of chapter-III is approach of PFC either low power or high power and mode of operation. Chapter-IV gives the idea of Parallel Power Flow Scheme with respect of conventional PFC scheme. Chapter-V discusses about Parallel Power Flow AC/DC converter. In the chapter-VI closed loop simulation is given. In Chapter-VII simulation design is given. At last conclusion is given in chapter-VIII.

## 2. POWER FACTOR CORRECTION TECHNIQUES

In recent years, single-phase switch-mode AC/DC power converters have been increasingly used in the industrial, commercial, residential, aerospace, and military environment due to advantages of high efficiency, smaller size and weight. However, the proliferation of the power converters draw pulsating input current from the utility line, this not only reduce the input power factor of the converters but also injects a significant amount of harmonic current into the utility line. To improve the power quality, various s have been proposed. There are harmonic as IEC 1000-3-2 introduced for improving power quality. By the introduction of harmonic norms now power supply manufacturers have to follow these norms strictly for the remedy of signal interference problem [5].

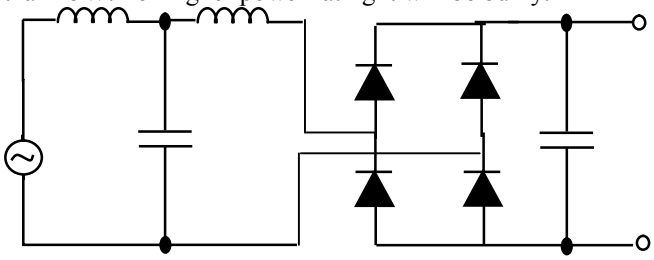
2.2 Classification of PFC Techniques

The various methods of power factor correction can be classified as:

1. Passive power factor correction techniques
2. Active power factor correction techniques

### 2.2.1 Passive Power Factor Correction Techniques

In this approach, an LC filter is inserted between the AC mains line and the input port of the diode rectifier of AC/DC converter as shown in Figure.2.1 [5]. This technique is simple and rugged but it has bulky size and heavy weight and the power factor cannot be very high. Therefore it is now not applicable for the current trends of harmonic norms. Basically it is applicable for power rating of lower than 25W. For higher power rating it will be bulky.



### 2.2.2 Active Power Factor Correction Techniques

The below flow chart shows the active power factor correction techniques.

In this approach, switched mode power supply (SMPS) technique is used to shape the input current in phase with the input voltage. Thus, the power factor can reach up to unity. Figure 2.2 shows the circuit diagram of basic active power correction technique. By the introduction of regulation norms IEC 1000-3-2 active power factor correction technique is used now a day. There are different topologies for implementing active power factor correction techniques. Basically in this technique power factor correcting cell is used for tracking the input current in phase of input voltage such that input power factor come up to unity. Comparing with the passive PFC techniques, active PFC techniques have many advantages such as, high power factor, reduced harmonics, smaller size and light-weight. However, the

complexity and relatively higher cost are the main drawbacks of this approach [5].

2.3 Classification of Active Power Factor Correction Techniques

The active PFC techniques can be classified as:

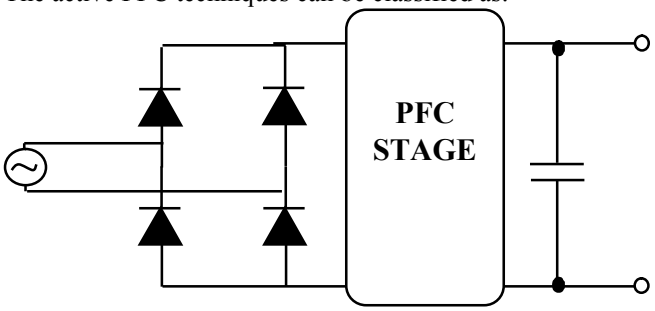



**Figure 2.2: The Active Power Factor Correction Technique**

1. PWM power factor correction techniques
2. Resonant power factor correction techniques
3. Soft switching power factor correction techniques

### 2.3.1 PWM Power Factor Correction Techniques

In this approach, the power-switching device operates at pulse-width-modulation mode. Basically in this technique switching frequency of active power switch is constant, but turn-*ON* and turn-*OFF* mode is variable. The advantages are simple configuration, ease of analysis and control, lowest voltage and current stress. Therefore it is extensively used in PFC circuits. For the minimization of converter size PWM technique generates significant switching loss [6].

Different topologies of PWM techniques are as follows:

1. Buck type
2. Boost type
3. Flyback type
4. Forward type

#### *2.3.1.1 Buck Type PWM Power Factor Correction Topology*

The buck, or step down, converter converts an input voltage to a regulated, lower-valued, output voltage. A simplified circuit diagram and associated operating waveforms are shown in Figure 2.3. In this circuit, with power switch $S_1$, closed, inductor current ($I_{L1}$) builds up linearly at a rate approximately equal to ($V_{IN} - V_{OUT}$) /$L_1$. The inductor current flows into the load ($R_L$) and the output capacitor ($C_1$).

As the voltage across $C_1$ rises out of the PWM's upper regulation tolerance window, $S_1$ opens and terminates the current flow from the input voltage source. Even with $S_1$ open, the current still flows in $L_1$ and is "caught" by the rectifier diode $D_1$. The inductor current now decreases linearly at a rate approximately equal to $V_{OUT}$/ $L_1$. When the voltage across capacitor $C_1$ falls out of the PWM's lower regulation tolerance window, $S_1$ closes and the cycle repeats.

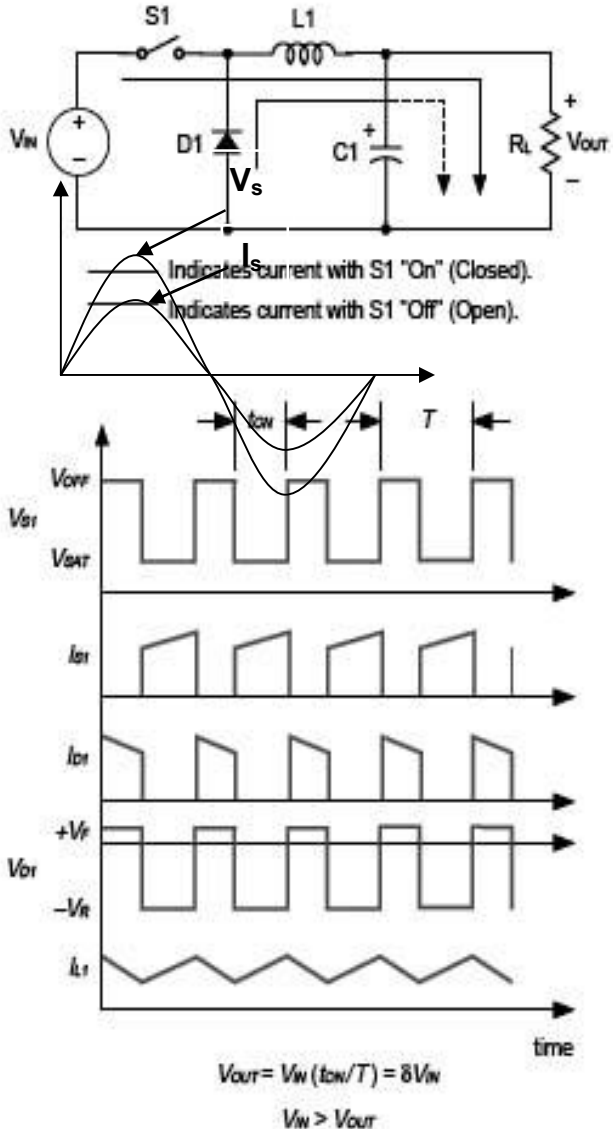



**Figure 2.3: The Buck Type PWM PFC Topology and waveforms**

The input-to-output transfer function can be derived by equating the inductor volt-second product (the energy) during the "on" time to the volt-second product during the "off" time. These two products should be equal in order to satisfy conservation of energy. The on-time energy is given by: $E_{ON} = (V_{IN} - V_{OUT})\ t_{ON}$, and the off-time energy is given by: $E_{OFF} = (V_{OUT})\ t_{OFF}$, where $t_{OFF} = T - t_{ON}$. Substituting yields:

$(V_{IN} - V_{OUT})t_{ON} = V_{OUT}\ (T - t_{ON})$

$(V_{IN})t_{ON} = (V_{OUT})T$

$V_{OUT} = V_{IN}(t_{ON}/T)$, $t_{ON}/T$ = *duty cycle* ($D$)

$V_{OUT}/V_{IN} = D$

The advantage of buck type topology is that the converter can supply a low output voltage with respect to input voltage. The disadvantages are, significant current distortion, EMI is higher because discontinuous input current so filter design is costly. Basically, it is a basic DC-DC converter and it is not used for power factor correction [5], [6].

#### *2.3.1.2 Boost Type PWM Power Factor Correction Topology*

The boost, or step up, converter converts an input voltage into a regulated, greater-valued, output voltage. A simplified circuit diagram and associated operating waveforms are shown in Figure 2.4. In this circuit, with power switch $S_1$ closed,inductor current ($I_{L1}$) builds up linearly at a rate approximately equal to $V_{IN}/ L_1$. During this time, load current (through $R_L$) is drawn from output capacitor $C_1$. As the voltage across $C_1$ drops out of the PWM's lower regulation tolerance window, $S_1$ opens and stops shunting input current. Even with $S_1$ open, the current still flows in $L_1$ and is "caught" by rectifier diode $D_1$. The current is now steered into the load circuit ($C_1$ and $R_L$). The inductor current now decreases linearly at a rate approximately equal to $(V_{OUT} - V_{IN})/L_1$, and when the voltage across capacitor $C_1$ rises above the PWM's upper regulation tolerance window, $S_1$ closes and the cycle repeats.

For the input-to-output transfer function, the on-time energy is given by: $E_{ON} = (V_{IN})\ t_{ON}$, and the off-time energy is given by: $E_{OFF} = (V_{OUT} - V_{IN})t_{OFF}$, where $t_{OFF} = T - t_{ON}$. Substituting yields:

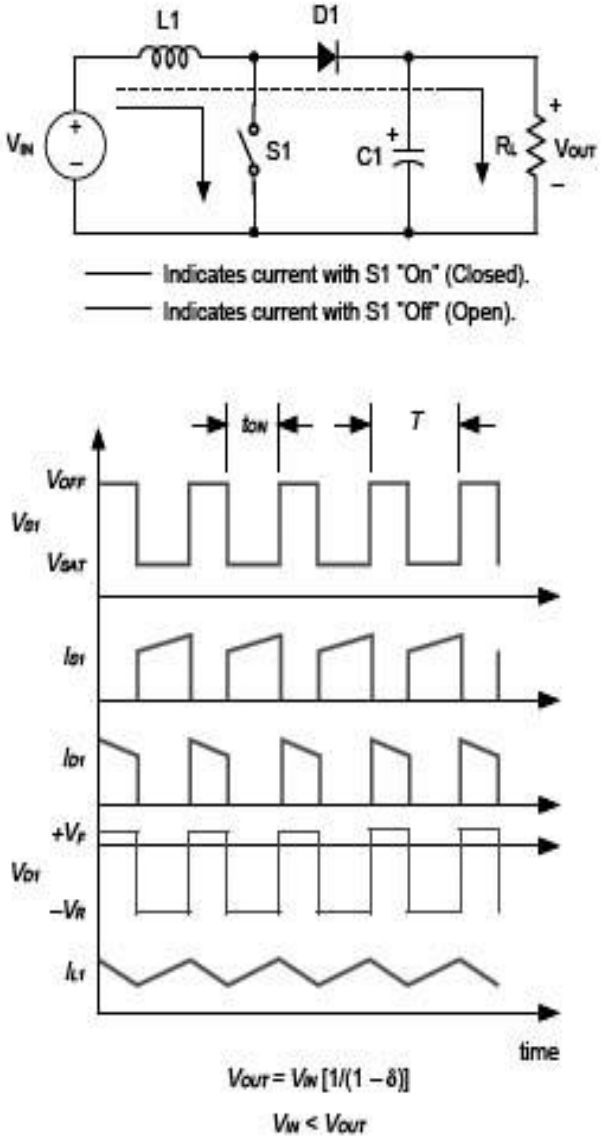



**Figure 2.4: The Boost Type PWM PFC Topology and waveforms**

$(V_{IN})\ t_{ON} = (V_{OUT} - V_{IN})\ (T - t_{ON})$

$(V_{IN})T = V_{OUT}\ (T - t_{ON})$

$V_{OUT} = V_{IN}\ (T/(T - t_{ON}))$

$V_{OUT} = V_{IN}\ (1/\ (1 - D))$

$V_{OUT}/V_{IN} = 1/\ (1 - D)$

Advantages of this topology are current mode control is easy and less EMI so reduced input filtering requirements. The main disadvantages are more conduction loss, no isolation and output voltage is always higher than input voltage [5], [6].

***2.3.1.3 Flyback Type PWM Power Factor Correction Topology***

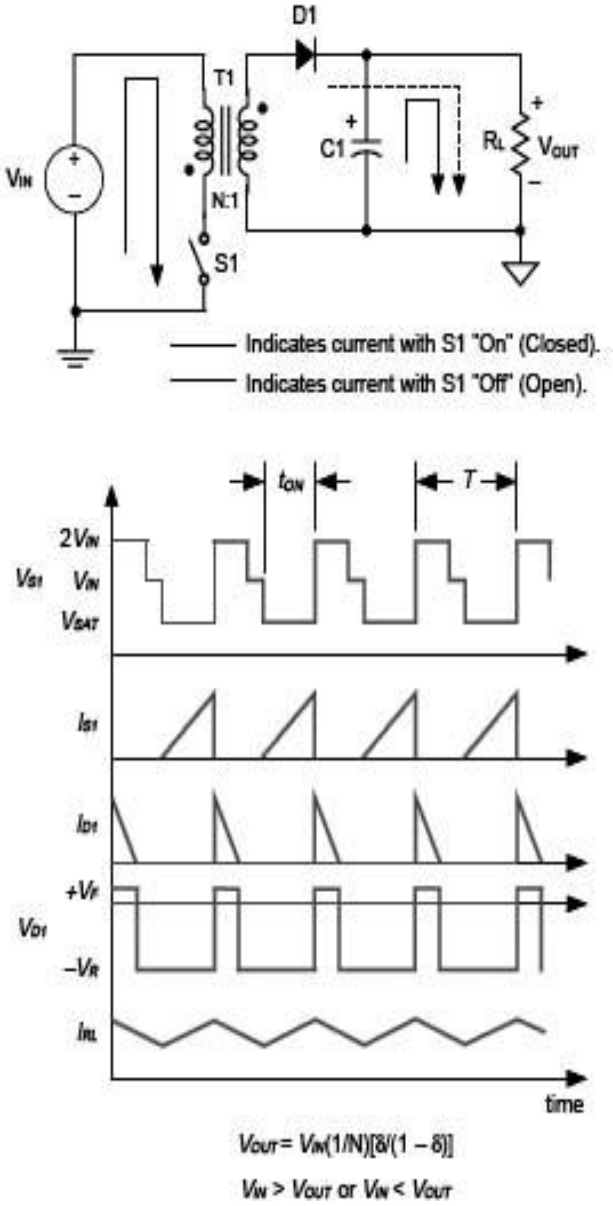



**Figure 2.5: The Flyback Type PWM PFC Topology and waveforms**

The flyback converter converts an input voltage into a regulated, lower or higher-valued output voltage depending on its transformer's turns ratio. A simplified circuit diagram and associated operating waveforms are shown in Figure 2.5. In this circuit, with power switch $S_1$ closed primary

current ($I_{S1}$) builds up linearly at a rate approximately equal to $V_{IN}$/ L (primary). During this time, because of the phasing of the transformer (more aptly referred to as a coupled inductor), no energy (current) is supplied to the load by the transformer secondary. Load current, during this interval, is supplied by $C_1$.

As the voltage across $C_1$ falls below the PWM's lower regulation tolerance window, $S_1$ opens and terminates the current flow from the voltage source. When $S_1$ opens, the magnetic field in the transformer collapses, and the voltages at the primary and secondary undergo a polarity reversal. The energy in the primary is now available to the secondary, and secondary current flows and decreases linearly at a rate approximately equal to $V_{OUT}$/L (secondary).When the voltage across $C_1$ rises above the PWM's upper regulation tolerance window, $S_1$ closes and the cycle repeats.
Concerning the input-to-output transfer function, the on-time energy is given by: $E_{ON} = (V_{IN}/N)\ t_{ON}$, and the off-time energy is given by: $E_{OFF} = (V_{OUT})\ t_{OFF}$, where $t_{OFF} = T - t_{ON}$ and $N$ is the transformer's turns ratio.
Substituting yields:
$(V_{IN}/N)t_{ON} = V_{OUT}\ (T - t_{ON})$
$(V_{IN})\ t_{ON} = NV_{OUT}\ (T - t_{ON})$
$V_{OUT} = (V_{IN})\ t_{ON} / (NT - Nt_{ON})$, $t_{ON}/T$ = duty cycle ($D$)
$V_{OUT}/V_{IN} = D/ (N - ND)$
$V_{OUT}/V_{IN} = (1/N)\ (D/ (1 - D))$
The disadvantages are higher switching device voltage and current rating, input current is discontinuous so requirement of careful design of input filter, difficult to program the input current with current mode control [5], [6].

#### *2.3.1.4 Forward Type PWM Power Factor Correction Topology*

The forward converter converts an input voltage into a regulated, lower or higher-valued output voltage depending on its transformer's turns ratio. A simplified circuit diagram and associated operating waveforms are shown in Figure 2.6. In this circuit, with power switch $S_1$ closed, transformer primary current $I_{S1}$ increases linearly at a rate approximately equal to $V_{IN}/L$ (primary). Also during this time, due to the input-to-output winding phasing of $T_1$, a voltage whose magnitude is $V_{IN}/N$ is present at the transformer's secondary winding. The secondary current (which flows through rectifier diode $D_1$ and output inductor $L_1$) increases linearly at a rate approximately equal to $(V_{IN}/N)/L_1$. This current also flows into the load $RL$ and the output capacitor $C_1$.

As the voltage across $C_1$ rises out of the PWM's upper regulation tolerance window, $S_1$ opens and terminates the current flow from the voltage source. When $S_1$ opens, the secondary winding undergoes a voltage phase reversal and no longer provides current through $D_1$. However, current still flows in $L_1$ and is "caught" by rectifier diode $D_2$. The inductor current now decreases linearly at a rate approximately equal to $V_{OUT}$/$L_1$, and when the voltage across capacitor $C_1$ falls out of the PWM's lower regulation tolerance window, $S_1$ closes and the cycle repeats.

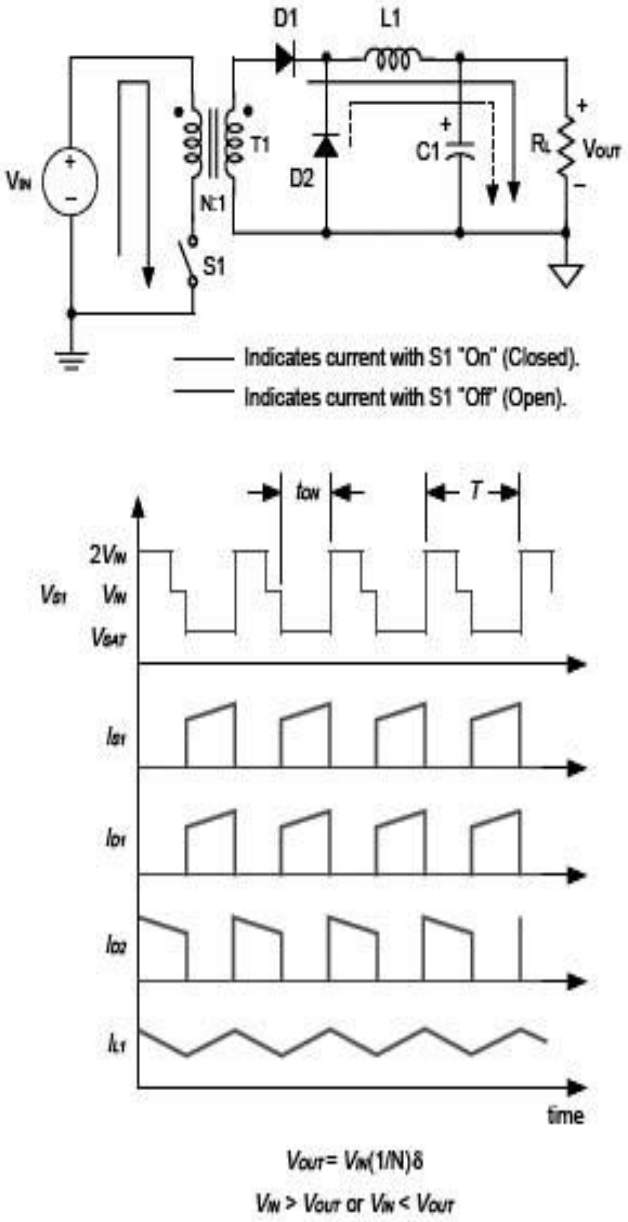



**Figure 2.6: The Forward Type PWM PFC Topology and waveforms**

In determining the input-to-output transfer function, the on-time energy is given by: $E_{ON} = (V_{IN}/N - V_{OUT})\ t_{ON}$, and the off-time energy is given by: $E_{OFF} = (V_{OUT})\ t_{OFF}$, where $t_{OFF} = T - t_{ON}$ and $N$ is the transformer's turns ratio. Substituting yields:
$(V_{IN}/N - V_{OUT})\ t_{ON} = V_{OUT}\ (T - t_{ON})$
$V_{OUT} = (V_{IN}/N)\ (t_{ON}/T)$
$V_{OUT}/V_{IN} = (1/N)\ D$

### 2.3.2 Resonant Power Factor Correction Techniques

In the resonant converter, the voltage across a switch or the current through a switch is shaped by the resonance of inductor and capacitor to become zero at the time of turned *ON* or *OFF*. Thus the switching loss is greatly reduced. The high power factor is achieved by the natural gain-boosting characteristic of the resonant converter. The major drawbacks are higher voltage and current stress on the

power switch with respect to PWM mode and variable switching frequency employed. Figure 2.7 shows a PFC circuit in which a resonant converter is inserted between the input diode rectifier and the dc-dc converter. This resonant converter can be series resonant converter [5], [6] or a charge pump resonant network [5], [7]. The advantage is that the current stress and voltage stress on resonant components as well as power switches are lower than the previous resonant converter.

**2.3.1.6 Soft Switching PFC Techniques**

The soft-switching PFC technique combines the advantages of PWM mode and resonant mode techniques [5].With an additional resonant network consisting of a resonant inductor, a resonant capacitor and an auxiliary switch [5], [6]. The AC/DC converter operates in PWM mode during most portion of a switching cycle but operates in resonant mode during the switch turn-*ON* and turn-*ON* intervals. As a result, the PFC circuit works at constant switching frequency and the power switch turns *ON* and *OFF* at zero current or zero voltage conditions. Thus efficiency and power factor both improved by this technique. Figure 2.8 shows boost PFC circuit with a soft switching network.

## 3. SINGLE PHASE ACTIVE POWER FACTOR CORRECTION

3.1 Introduction

Conventional *ON*-line power converters with diode-capacitor rectifier front-end have distorted input current waveform with high harmonic content. They cannot meet neither the European line-current harmonic regulations defined in the IEC1000-3-2 document or the corresponding Japanese input-harmonic current specifications. To meet the requirements of above norms it is customary to add a power factor corrector ahead of the isolated dc/dc converter section of the switching power supply. Again another dc/dc converter is needed for output voltage regulation. Thus there are two converter is needed for single-phase active power factor correction for the requirement of high input power factor and tight output regulation.

There are two approaches for single-phase active power factor correction:

1. two-stage approach
2. single-stage approach

3.2 Two-Stage Approach of Active Power Factor Correction

Two-stage approach is commonly used approach in high power applications [8]. The block diagram of two stages PFC converter is shown in Figure.3.1. In this approach, there are two independent power stages. The front-end PFC stage is usually a boost or buck-boost (or flyback) converter. The dc/dc output stage is the isolated output stage that is implemented with at least one switch, which is controlled by an independent PWM controller to tightly regulate the output voltage. The two-stage approach is a cost-effective approach in high power applications; its cost-effectiveness is diminished in low-power applications due to the additional PFC power stage and control circuits.

3.3 Single-Stage Approach of Active Power Factor Correction.

A single-stage scheme combines the PFC circuit and DC/DC power conversion circuit into one stage. A number of single-stage circuits have been reported in recent years [8]. Figure 3.2 shows the block diagram of single-stage approach. Compared to the two-stage approach, the single approach uses only one switch and controller to shape the input current and to regulate the output voltage. Although for a single-stage PFC converter attenuation of input-current harmonics is not as good as for the two-stage approach. But it meets the requirements of IEC1000-3-2 norms. Again it is cost effective and compact with respect to two stage approach.

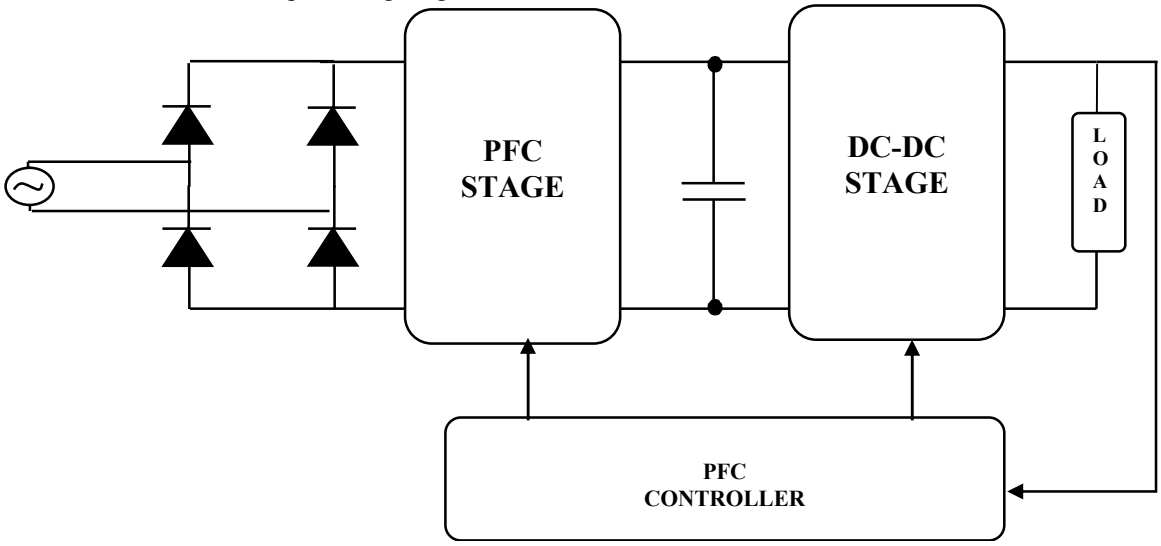



**Figure 3.2: The Block Diagram of Single-Stage PFC Converter**

There are four possible combinations to obtain different single stage single switch PFC converters [9]:

1. Discontinuous Conduction Mode PFC + Continuous Conduction Mode DC/DC
2. Discontinuous Conduction Mode PFC + Discontinuous Conduction Mode DC/DC
3. Continuous Conduction Mode PFC + Continuous Conduction Mode DC/DC

4. Continuous Conduction Mode PFC + Discontinuous Conduction Mode DC/DC

## 4. PARALLEL POWER TRANSFER SCHEME

4.1 Introduction

Either in two-stage or single-stage of single phase PFC the input power is processed twice to reach the output [10]. There are two functional cells known as PFC cell and DC/DC cell is used for power factor correction and output voltage regulation respectively. Figure 4.1 shows the parallel power processing in typical single-phase single-stage approach by block diagram. Suppose efficiency of PFC cell is $\eta_1$ and DC/DC cell is $\eta_2$, then the output power will be

$$P_o = P_{in}\eta_1\eta_2 \quad (4.1)$$

Thus the efficiency of single-stage AC/DC converter will be

$$\eta = \eta_1\eta_2 \quad (4.2)$$

Thus the twice power processing approach means low conversion efficiency because it is a product of two fraction. So, advancement is needed for the improvement of conversion efficiency.

The new approach come into picture according to that, it is not necessary to process all input power twice to achieve well-regulated and high input power factor and DC output power. In this approach power is processed only once to keep the total DC output power constant. Figure 4.2 shows the proposed new parallel power flow scheme. [11]. Let $k$ portion of power from input goes through DC-DC converter, and remaining $(1-k)$ power through PFC cell. Based on this concept, output power can be obtained by Eqn.4.3.

$$P_o = P_{in}\left(k\eta_1 + (1-k)\eta_2\right) \quad (4.3)$$

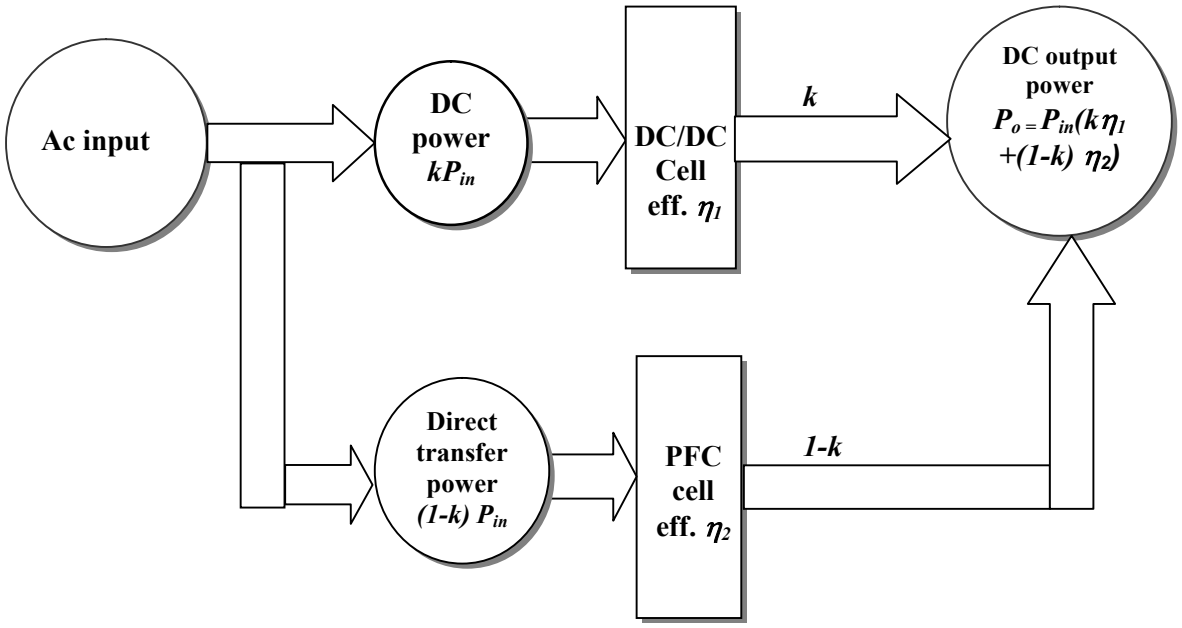



**Figure 4.2: Parallel PFC Scheme**

Thus efficiency of proposed parallel power transfer scheme single-stage PFC AC/DC converter is,

$$\eta = \left(k\eta_1 + (1-k)\eta_2\right) \quad (4.4)$$

Comparing Eqn.4.2 and Eqn.4.3, it is easy to say efficiency of Parallel Power Flow scheme is more than the efficiency of conventional energy transfer scheme.

4.2 Paralleling Techniques

Paralleling of converter power modules is a well-known technique that is often used in medium-power applications to achieve the desired output power with smaller size power transformers and inductors [12]. Since magnetics are critical components in power converters because generally they are the size-limiting factors in achieving high-density and/or low-profile power supplies, the design of magnetics becomes even more challenging for high-power applications that call for high power-density and low-profile packaging. Instead of designing large-size centralized magnetics that handle the entire power, low-power distributed high density/low-profile magnetics can be utilized to handle the high processing power, while only partial load power flow through each individual magnetics [12, 13].

In addition to physically distributing the magnetics and their power losses and thermal stresses, paralleling also distributes power losses and thermal stresses of the semiconductors due to a smaller power processed through the individual paralleled power stages. As a result, paralleling is a popular approach to eliminating "hot spots"

in power supplies. In addition, the switching frequencies of paralleled, lower-power power stages may be higher than the switching frequencies of the corresponding single, high-power processing stages because lower-power, faster semiconductor switches can be used in implementing the paralleled power stages. Consequently, paralleling offers an opportunity to reduce the size of the magnetic components and to achieve a low-profile design for high power applications.

Without increasing the number of power stages and control-circuit components, the transformer magnetics can be distributed by direct transformer paralleling. Not only that transformer paralleling distributes the processed power in each magnetics components, but also their power losses and thermal stresses are distributed at the same time. However, current sharing among the paralleled transformers needs to be maintained to ensure power balance.

In its basic form, the interleaving technique can be viewed as a variation of the paralleling technique, where the switching instants are phase-shifted within a switching period [14]. By introducing an equal phase shift between the paralleled power stages, the total inductor current ripple of the power stage seen by the output filter capacitor is lowered due to the ripple cancellation effect [14].

## 5. Results

The circuits shown in Figure.5.1 and 2.5 have been simulated in MATLAB/SIMULINK, the simulation results is shown in Figure. [5.1-5.4]. the operating switching frequency is 37 kHz. In proposed system, forward converter acts as voltage regulator with PI controller gives constant output voltage and flyback converter with hysteresis controller makes input current to be sinusoidal. In figure 5.1 input current tracks the input voltage so input power factor is almost unity. As shown in Figure.5.1, output voltage is fixed at 48V, with a ripple of .43V, so it is well regulated and load current is also shown. In Figure 5.2, the output power of load is almost equal at 200w. In figure 5.4 shows the output voltage ripple. In figure 5.5 shows the simulink implementation of flyback converter used for power factor control and voltage regulation. As it is an inherently power factor corrected circuit so only PI controller for voltage regulation is being used. Figure 5.6 shows input current tracks the input voltage so input power factor is almost unity but it has high THD as compared to parallel power scheme. As shown in Figure.5.7, output voltage is fixed at 48V, with a ripple of .3V, so it is well regulated. In Figure 5.8, the output power of load is almost equal at 200w. In figure 5.9 shows the output voltage ripple.

**SIMULATION DATA OF PARALLEL POWER FLOW SCHEME**

INPUT VOLTAGE ($V_{in}$) = 150 $V_{RMS}$
OUTPUT VOLTAGE ($V_O$) = 48 V
OUTPUT POWER (Po) = 200 W
SWITCHING FREQUENCY (fsw) = 37 kHz
TRANSFORMER TURNS RATIO (n) = 4.41:1

***DC/DC CELL***

POWER RATING = 109.4[W]
MAGNETIZING INDUCTANCE (Lmp)= 0.5 [mH]
OUTPUT CAPACITOR (Co) = 1500[µF]
DC BUS CAPACITOR (Cp) = 660[µF]
INPUT INDUCTOR (Ldr) = 600[µH]
OUTPUT INDUCTOR (Lf) = 5[µH]

***PFC CELL***

POWER RATING = 90.6 [W]
MAGNETIZING INDUCTANCE (Lmh) = 1.2 [mH]

**SIMULATION DATA OF FLYBACK CONVERTER**

INPUT VOLTAGE ($V_{in}$) = 150 $V_{RMS}$
OUTPUT VOLTAGE ($V_O$) = 48 V
OUTPUT POWER (Po) = 200 W
SWITCHING FREQUENCY (fsw) = 37 kHz
TRANSFORMER TURNS RATIO (n) = 4.41:1

**COMPARISON BETWEEN PARALLEL POWER SCHEME AND SINGLE CONVERTER**

| | Parallel Power flow converters | Single forward converter |
|---|---|---|
| Total Harmonic Distortion (THD). | .34% | 1.2% |
| Efficiency(ή) | 89.79% | 85.70% |
| Dc link Capacitance(Cp) | 1320 micro farad | 1320 micro farad |
| Output Capacitance(Co) | 1500 microfarad | 1600 microfarad |
| Input Inductance($L_{dr}$) | 500 micro Henry | 1850 micro Henry |
| Output voltage Ripple | .9%(.4v) | .7%(.3v) |

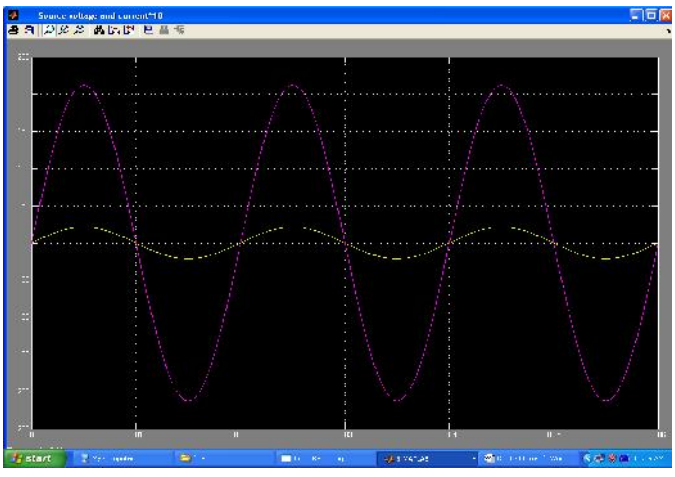


**Figure 5.1 Input current tracking the input voltage**

**Figure 5.2 Output voltage and current**

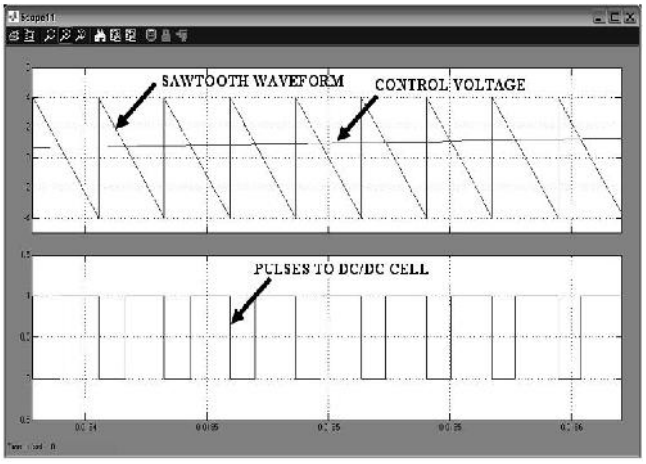



**Figure 5.5**

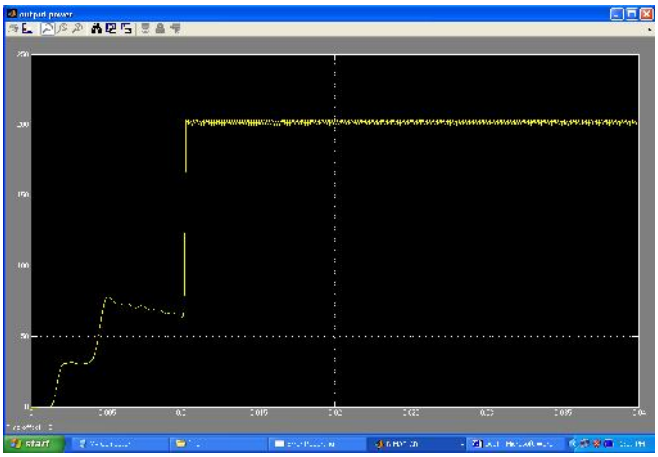


**Figure 5.3 Output power**

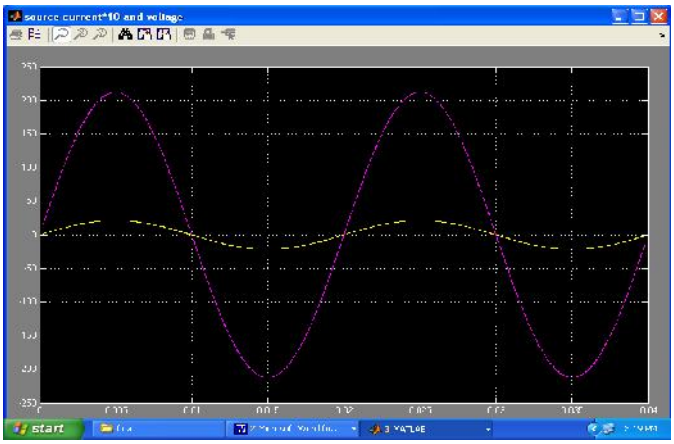


**Figure 5.6 Input current tracking input voltage**

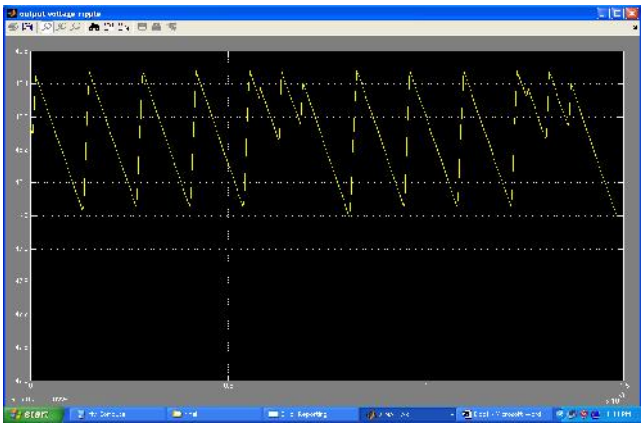


**Figure 5.4 Output voltage ripple**

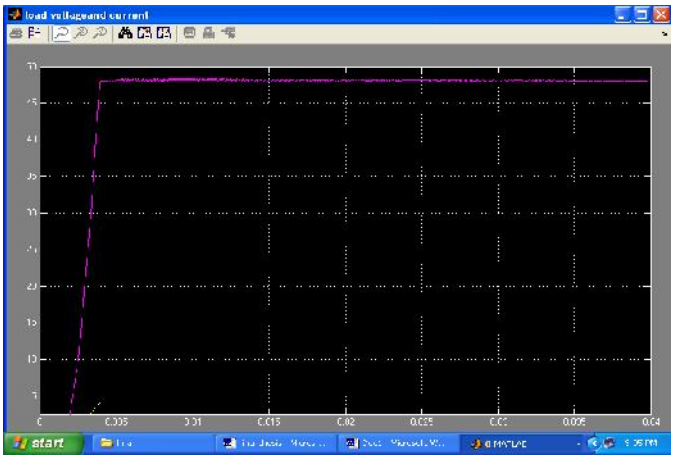


**Figure 5.7 Output voltage and current**

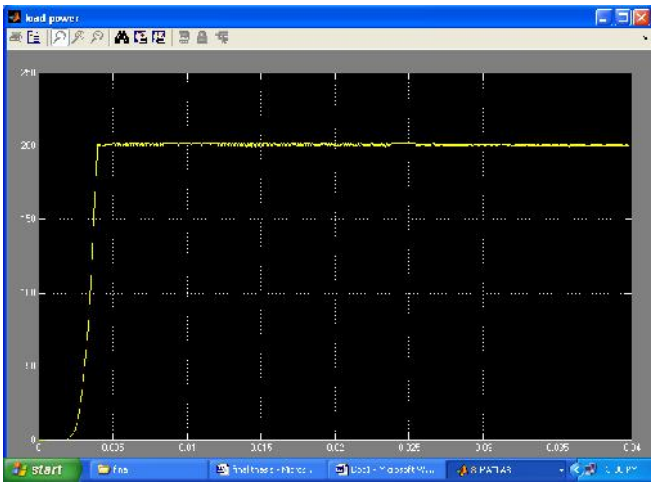


**Figure 5.8 Load power**

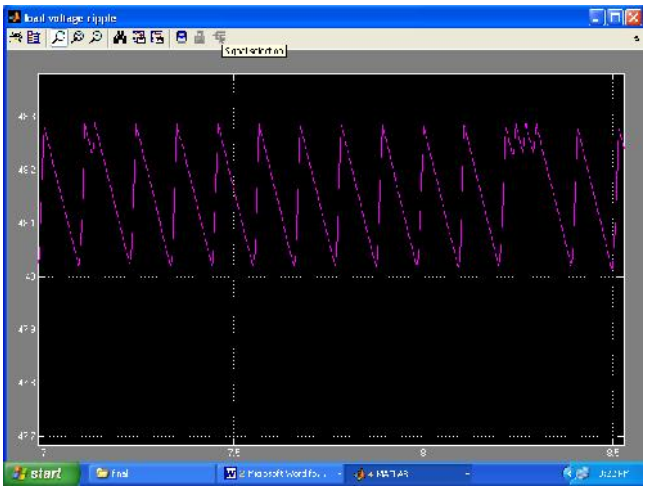


**Figure 5.9 Load voltage ripple**

## 6. CONCLUSIONS AND FUTURE WORK

From the discussions in this report, it is clear that the power factor correction is being given significant importance for low and medium power applications. Also as power electronic equipments are increasingly being used, they pose a serious problem of low order harmonics on utility side. Among various schemes available for PFC, the single stage scheme is best suited for low and medium power application because of its cost effectiveness, small component size. But in this scheme, there is a serious limitation of high dc link voltage rise under light load condition. This problem can be addressed by using the concept of Parallel Power Flow Concept.

From the simulation results of Parallel Power Flow topology, it is clear that parallel processing of power is an effective way to control high dc link voltage and hence reduces the component stresses. This topology also maintains a high input power factor and a tight output voltage regulation without compromising with high DC bus voltage. Moreover, the efficiency of overall power conversion is high.

Input voltage = 150 $V_{P-P}$
Load voltage = 48 V
Output ripple voltage = 40 mV
Load current = 4.16A
Power factor = 0.9973
THD = 0.34%
Overall Efficiency =89.79%.

From the above discussions it is concluded that the Parallel Power Flow Approach is best suited for the power factor correction and results show the performance.

The future work comprises of

1. Hardware implementation to be done to compare the results.
2. Control loop can be implemented in different ways such as, Conventional PI controller, DSP based controller and by incorporating a DAQ card along with MATLAB/Real-Time Workshop or Lab VIEW for system interaction.
3. Implementation of optimization techniques in design will be more cost effective and compact.
4. Controller can be compared with soft computing techniques such as Fuzzy Logic Control, Neural Network control and Neuro-Fuzzy control.

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