Stuck- at Fault Detection in Combinational Network Coefficients of the RMC with Fixed Polarity (Reed-Muller Coefficients)

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Abstract: **The paper presents a new method for computing all 2" canonical Reed-Muller forms(RMC forms) of a Boolean function and fixed polarity matrix method. The method constructs the coefficients directly and no matrix multiplication is needed. It is also usable for incompletely specified functions and for calculating a single RMC form. The method exhibits a high degree of parallelism. A fault we mean, in general any change in the value of an element with respect to its nominal value which can cause the frailest of the whole circuit. In the stuck-at model it is generally assume that a logic input or output is static or fixed to either logic '1'(stuck-at one) or logic '0' (stuck-at zero) and abbreviated as s-a-0 and s-a-1 respectively.**

Keywords: ***Fault detection, Read Muller Coefficients, Boolean function.***

I- INTRODUCTION

Digital systems are becoming increasingly complex and sophisticated development in LSI/VLSI technology which has allowed not only higher package density but also made ,it feasible to implement additional peripheral support devices that were earlier interconnected externally .in addition it permitted on-chip in corporation of novel advanced features such as self testing , supervisory and fail-safe etc. and hence simplified the task of design and maintenance of complex systems by reducing external interconnecting lines as also thought improved reliability. Many digital hardware building blocks such as Encoders/ Decoders, ROM / Demux, ROMs, PLAs and ASICs are frequently use to generate multiple output combinational function to implement digital systems intended for various application areas such as DSP, Automation , Control and computer systems etc. The increasing use digital systems in all aspects of social, economic and industrial applications have necessitated developed.

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II- METHOD FOR FAULT DETECTION:

Most commonly four methods are for used

1. Fault table method,

2. Boolean difference method

3. Path sensitization method and

4. D-algorithm

The advantage of this representation is the fact that the resulting circuit needs at most n inputs in contrast to up to 2n inputs in other cases. The second essential advantage is the fact that for each function represented in RMC form there exists circuit, which can be tested with maximum 3n + 4 tests, most of them independent of the realized function [2]. It is easy to see that for a Boolean function with n variables there exist 2" different RMC forms. Each of these forms can be characterized by 2" Boolean values a, indicating the presence or the absence of a given product term.

The aim is now to find the RMC form with the least number of a, = 1. Algorithms existing up to now build up a 2" x 2" matrix, called polarity-matrix [7], where every coefficient a, of each of the 2" polarities is given. This polarity-matrix is constructed using matrix multiplication [3], which means that these algorithms

Belong to the class with complexity AT2 = O (16") [I 3]

Method:

Definition: Let T n be a 2n x2n binary matrix. T n will recursively be defined as.

$$Tn = \begin{bmatrix} t^{n-1} & 0 \\ t^{n-1} & t^{n-1} \end{bmatrix} \quad \text{And To= [l]}$$

It becomes apparent that the same matrix can be obtained by the nth Kronecker-power [12] of T'.

Definition:

Consider a Boolean function f given as

$$[f] = [f', f'']$$

Where, $[f'] = [f0 ,\ldots\ldots,f\, 2^{n-1}-1]$

And, $[f''] = [f\, 2^{n-1},\ldots.,f\, 2^{n-1}]$

Then $2^n \times 2^n$ matrix B[f] is define as $B[F] = \begin{bmatrix} B[F'] & B[F''] \\ B[F''] & B[F'] \end{bmatrix}$ and B[fi] =fi

Let z^n be the nth kronecker power of $Z' = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}$

Then m[f] =B[f].2 z^n

$$\begin{bmatrix} P[0\,0\,1\,0] & P[1\,1\,1\,1] \\ P[1\,1\,0\,1] & P[1\,1\,1\,1] \end{bmatrix} =$$

$$\begin{bmatrix} P[00] & P[10] & P[11] & P[00] \\ P[10] & P[10] & P[11] & P[00] \\ P[11] & P[10] & P[11] & P[00] \\ P[01] & P[10] & P[11] & P[00] \end{bmatrix} =$$

$$\begin{bmatrix} 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}$$

w1	3	4	3	3	3	5	2	3
a0	1	0	1	0	1	1	1	1
a1	1	1	1	1	0	0	0	0
a2	0	0	0	0	0	1	0	1
a3	0	0	0	0	1	1	1	1
a4	0	1	0	0	0	1	0	0
a5	1	1	0	0	1	1	0	0
a6	0	1	0	1	0	1	0	1
a7	1	1	1	1	1	1	1	1
w2'	4	5	3	3	4	7	4	5
w2	2	4	1	2	2	5	2	4
W=∑ wi	8	11	9	9	7	13	7	10

That computation of the coefficients of the RMC forms off for a given polarity is possible without constructing the whole matrix P. This can be advantageous in cases of lack of storage The 3-output
Polynomials with polarity (000) are as follows:
f0 = X1 ⊕XOX1⊕X2⊕ X0X1X2X3

f1 = X1 ⊕XOX1⊕X2⊕ X0X1⊕ XOX2X3

f2 = 1⊕X0⊕X0X2⊕ X0X2⊕ XOX1X3

P is an automorphism, because

P[f'] / P[f''] = P[f' / f''] = P[f''']

P is defined as above, then P[f]=m[f]

P[f]=P[0 0 1 0 1 1 0 1

Inputs			Outputs		
X2	X1	X0	f1	F2	f0
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	1	1	1
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	0	0

TABLE-1 The number of Ex-OR gates for the example

POLARITY MATRIX FOR FUNCITONS F0, F1 & F2

P =	0	1	2	3	4	5	6	7
a0	0	0	1	0	1	1	0	0
a1	0	0	1	1	0	0	0	0
a2	1	0	1	0	1	1	1	1
a3	1	1	1	1	0	0	0	0
a4	1	1	1	0	1	1	1	0
a5	0	0	1	1	0	0	1	1
a6	0	1	0	1	0	1	0	1
a7	1	1	1	1	1	1	1	1
w0'	4	4	7	5	4	5	4	4

w0	3	3	5	4	2	3	3	3
a0	0	0	1	0	0	1	1	0
a1	0	0	1	1	1	1	1	1
a2	1	0	1	0	1	1	1	1
a3	1	1	1	1	0	0	0	0
a4	0	1	0	0	0	1	0	0
a5	1	1	0	1	1	1	0	0
a6	0	1	0	1	0	1	0	1
a7	1	1	1	1	1	1	1	1
W1’	4	5	5	4	4	7	4	4

Table.multipleoutputw'i denotes the number of nonzero coefficients of the ith polynomial, referred to as the weight of the ith polynomial, and wi denotes the number of exclusive-OR gates for realization of the ith polynomial.

Polarity	000 x2x1x0	001 x2x1x0	010 x2x1x0	011 x2x1x0	100 x2x1x0	101 x2x1x0	110 x2x1x0	111 x2x1x0
W_0	2	4	1	2	2	5	2	4
W_1	3	4	3	3	3	5	2	3
W_2	3	3	5	4	2	3	3	3
$W=\sum w_1$	8	11	9	9	7	13	7	10
$W^{(3)}$	0	2	1	2	0	3	0	2
$W^{(2)}$	2	1	2	1	1	1	1	1
Ns	2	5	4	5	1	7	1	5
N_{exor}	6	6	5	4	6	6	6	6

TABLE 2. The No. of NOT, AND & Ex-OR gates for the example

We see that the polarity (011) requires 4 Ex-Or gates for realization of the 3-output functions with regard to the common terms which is minimum than other polarity, hence polarity, hence polarity 3(011) is the optimum one. The number of input NOT gates, output NOT gates and EX-OR gates.

Polarity	000	001	010	011	100	101	110	111
N_{in}	0	1	1	2	1	2	2	3
N_{out}	1	0	3	0	2	3	2	0
N_{not}	1	1	4	2	3	5	4	3
N_{and}	3	4	3	4	3	4	3	4
N_{exor}	6	6	5	4	6	6	6	6

Table: 3-output function

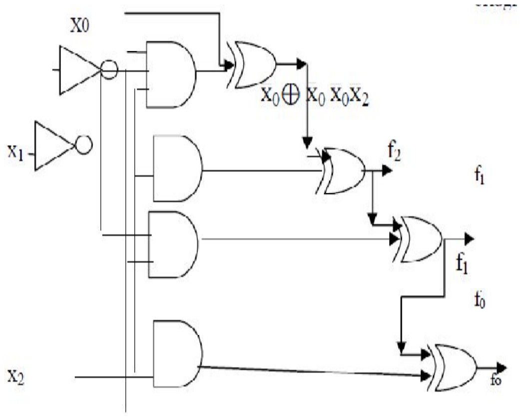

Fig : logical circuits for the example

III- PROPOSAL FOR FAULT DETECTION IN MULTIPLE OUTPUT CIRCUITS;

To detect the single/ multiple stuck-at- faults and bridging faults in multiple output systems, Its is proposed that above mentioned faults can be detected by verifying only one output function which contains all the input variables. If all the input variables do not appear in any of the output functions, then more than one function should be verified for fault detection. According to the proposal the faults in multiple output combinational circuit can be detected by considering the following cases.

Case1; When any one output function contains all input variables, then by testing only that function we can detect single/ multiple stuck-at faults and single bridging fault of n input circuit by verifying at most n, RM coefficients. The saving of test sets and time is highest in this case.

Case II;When in all output functions some input variables do not appear than we have to test more than one functions so that all input variables may be involved in fault detection. In this case larger test sets and computations have been claimed than in the case-1.

Case-III; When all the output functions are disjoint i.e., all functions have different input variables. Then all functions will be tested separately. It is the worst case in which largest test vectors and computations are required.

It has been reported that any R.M. network with k output and n input ($k \leq 2n$) requires at most 3n+5 test patterns to detect all single stuck-at faults and both AND and OR bridging faults which are detectable.

Concluding remarks:

a new method for the polarity matrix which is used for minimization of RMC forms of Boolean function is presented. It can be used for fully specified and incomplete specified functions.

In place of R. M. spectral coefficients techniques of fault detection, a more faster technique can be proposed to reduce further test sets and hardware overhead

P[f] matrix may be generated with further less no. of iterations, by modifying generation process of it.

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