Design and Implementation of Low Voltage, High Bandwidth MOS Current Mirrors

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Abstract: Design of current mirrors that can operate at higher frequency ranges is an important and growing field. This paper presents a modification to the conventional current mirrors, in the form of a precisely controlled resistance between the gates of the MOSFETs in order to achieve current mirroring at higher frequencies. Both passive and active realization techniques for the resistance have been considered in the improved current mirror. Likewise, to facilitate the operation of a current mirror at lower biasing voltages at the output, level-shifter technique has also been implemented.

I. Introduction:

In the typical IC design, biasing is often achieved by using a constant current source. Usually, this current is obtained by using a MOSFET biased to saturation, but generating separate drain currents whose values are free of process and temperature dependencies is not possible even if a known gate to source voltage is used[1]. Hence this is achieved by generating one constant and reliable current source and copying its value at different locations in the circuit. Current mirrors are employed for this purpose. Not only do they find extensive applications in almost all analog and mixed mode circuitry, their applications in analog signal processing circuits in communication systems[2] make improvement of their bandwidth an important field of study.

A Wilson current mirror is commonly used because of its good accuracy and output impedance[3]. Its operating bandwidth, although a bit higher than cascode configurations[4], can still be improved. A MOS Wilson mirror takes the circuit of Figure 2.

Applications of current mirrors in circuits operating at higher frequencies require suitable modifications because the present designs show high losses as the operating frequency is increased. In order to facilitate the use of mirrors at frequencies extending well into the microwave frequency ranges, a modification, in the form of a resistor between the gate terminals of the MOSFETs M1 and M2, has been considered. Level shifter configurations have been implemented for low voltage operation of mirrors.

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The paper is organized as follows. Section 1 deals with the simple current mirror and two modifications to it. A method for improvement of bandwidth for Wilson mirror has been presented in section 2. Section 3 presents low voltage operation circuit for a general and Wilson mirror.

1. Simple Current Mirror

A simple current mirror circuit replicates the input current of a current source and a current sink as the output current. However, the replication accuracy is poor due to channel length modulation effects. The bandwidth of this mirror is also very low.

It is a first order low-pass filter with its cut-off frequency given by[5]:

$$\omega_o = \frac{gm}{2Cgs} \quad \text{(i)}$$

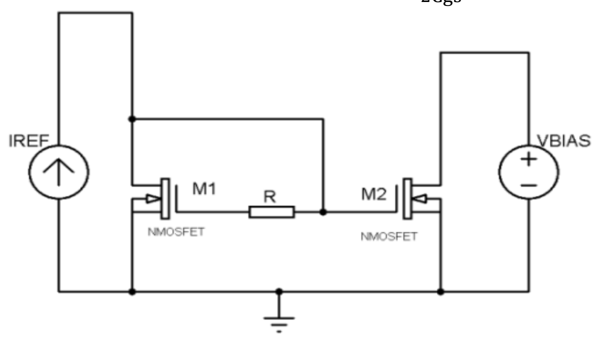

Figure 1

1. Passive Compensation: The introduction of a compensation resistor between the gates of M1 and M2 [6], as shown in Fig.1, transposes the first-order low-pass current mirror to a second-order low-pass mirror with one zero and two poles. The bandwidth is given as:

$$\omega_o = \sqrt{\frac{gm1}{RCgs1Cgs2}} \quad \text{(ii)}$$

   Thus by choosing $R=1/g_m$ and $C_{gs1}=C_{gs2}=C_{gs}$, the bandwidth is given as g_m/C_{gs} which is twice the bandwidth as compared to uncompensated current mirror.

2. Active Compensation: A diode-connected enhancement type MOSFET is used as an active compensation[7] resistance which tracks the trans-conductance which varies with process and temperature drifts.

2. High Frequency Response Of Wilson Current Mirror And Small Signal Model

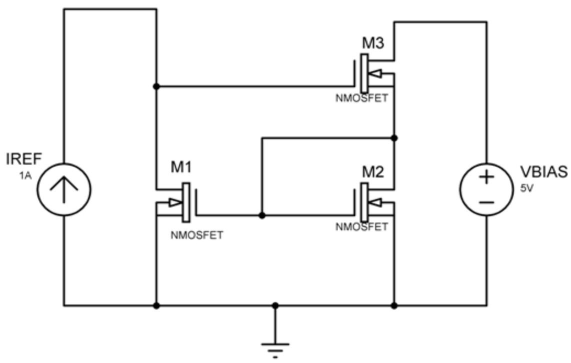

Figure 2

The transfer function of the general Wilson current mirror of Fig. 2, whose small signal model can be represented as in Fig. 3, can be obtained as:

$I_{out} = [\ g_{m2} + S(C_{gs1}+C_{gs2})\ ]\ V_{gs1}$

$V_{gs3}= (I_{ref}\text{-}g_{m1}V_{gs1}).\ \frac{1}{SCgs3}$

and, $I_{ref}= SC_{gs3}V_{gs3}+ g_{m1}V_{gs1}$

So, $\frac{Iout}{Iref} = \frac{[gm2+S(Cgs1+Cgs2)]Vgs1}{SCgs3Vgs3+gm1Vgs1}$ .... (iii)

and, $V_{gs3}= \frac{[gm2+S(Cgs1+Cgs2)]Vgs1}{gm3}$

which, upon substitution into (iii) yields,

$$\frac{Iout}{Iref} = \frac{S(Cgs1 + Cgs2) + gm2 * gm3}{S^2(Cgs1 + Cgs2)Cgs3 + SCgs3Cgs2 + gm1 * gm3}$$

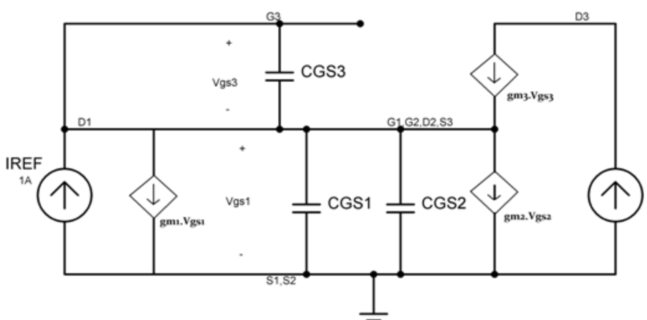

Figure 3

Hence this mirror is a second order low pass filter whose bandwidth is dependent on Cgs and the transconductance gm, and is given by:

$$\omega_o = \sqrt{\frac{gm1*gm3}{(Cgs1+Cgs2)*Cgs3}} \qquad \text{(iv)}$$

Making the assumption that process parameters are essentially equal for all transistors on a single chip, the expression for bandwidth reduces to:

$$\Omega_o= \frac{gm}{\sqrt{2}.Cgs} \qquad \text{(v)}$$

II. Enhancement of bandwidth

1. Passive compensation

Introduction of a resistance between the gate terminals of the MOSFETs M1 and M2 as shown in Fig.3 transforms the second-order low pass mirror into a third-order system with two zeros and three poles. The expression for output of the modified Wilson current mirror is given as:

$$\frac{Iout}{Iref} = \frac{S^2Cgs1Cgs2gm3R + S(Cgs1 + Cgs2)gm3 + gm2gm3}{S^3x + S^2(Cgs1 + Cgs2)Cgs3 + S(y) + gm1 * gm3}$$

where, x= Cgs1Cgs2Cgs3R and
Y= Cgs2gm1gm3R + gm2Cgs3

from which,

$$\omega_o^3 = \frac{gm1gm3}{Cgs1Cgs2Cgs3R}$$

$$\omega_{o}= \sqrt[3]{\frac{gm1*gm3}{Cgs1*Cgs2*Cgs3*R}} \qquad \text{(vi)}$$

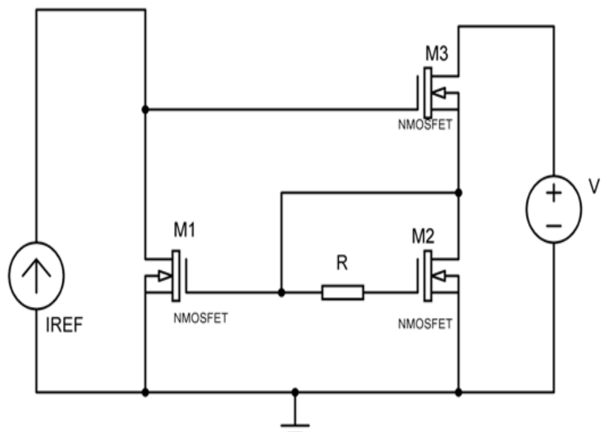

Figure 4

By selecting appropriate values of the resistance R, a considerable improvement in bandwidth can be achieved. For the value of $R= 1/g_m$,

$$\omega_o = \frac{gm}{Cgs} \qquad \text{(vii)}$$

2. Active compensation

Since a passive resistor is made of poly-silicon in full monolithic integration, its value has a large tolerance. Active compensation is used so that the resistor tracks the trans-conductance of MOSFETs, which varies considerably with process and temperature drifts. This resistor, realized using the diode connected MOS transistor, will result in minimal increase in chip area and minor increase in power consumption. This also allows for significant control over the precision of the value of the resistance by varying the aspect ratio of the compensating MOSFET only. The resultant circuit is the final modified Wilson current mirror with active compensation, shown in Fig.5.

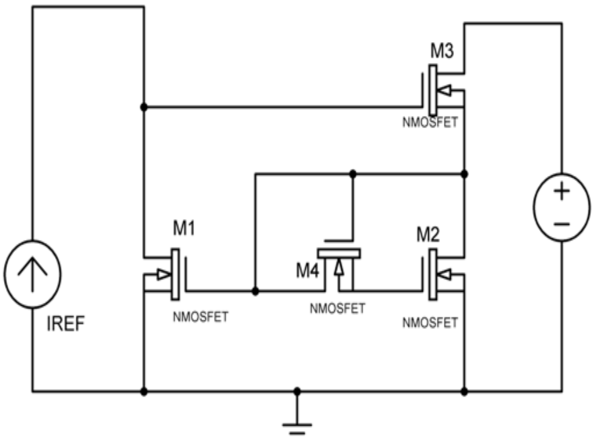

Figure 5

The previously assumed value of R= 1/gm is easily obtained here by from the MOSFET itself. Again, the expression obtained for 3dB frequency is same as before:

$$\omega_o = \frac{gm}{Cgs}$$

The value of gm can be modified to further improve the bandwidth of the mirror. This is only achieved at a compromise of chip size and area occupied by the circuit. Since using MOSFETs with channel widths beyond certain limits is unacceptable for the evolution of VLSI design, this may be achieved by using two or three MOSFETs in parallel in order to obtain higher desired values of g_m.

3. Low Voltage Analysis of the Wilson Current Mirror Using Level-shifter Technique.

Modern VLSI systems now operating from single 3.3V supplies and dropping, require high performance current mirrors that can operate with low voltages. The fact that the $V_{GS} - V_T$ of an MOS transistor determines most of its important parameters (e.g. g_m , w_o) has been used in some topologies to eliminate the dependence of the required minimal output voltage and hence increase the allowable signal swing[8]. This voltage drop (usually in the order of a volt) across the input terminal of those current mirrors may not be tolerable in all low-voltage applications. The use of current mirrors with low input voltage is especially important for implementation of VLSI test circuits which employ current sensing techniques. The level-shifter V_{GD}, can be implemented as shown in Figure. 6. The addition of a dc voltage source allows the MOSFETS to remain in saturation, hence requiring less bias voltage at the output.

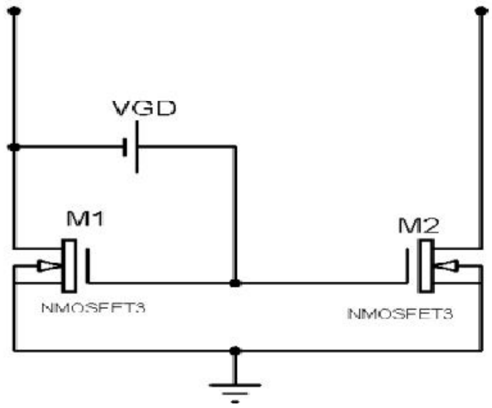

Figure 6

Suitable modifications to this circuit will need to be made, since producing a consistent voltage source V_{GD} is not a proper option. One of the means by this can be done is by using a PMOS in place of the voltage source, the gate of which is controlled by the input current itself. The analysis results have been compiled in the form of a table and simulation charts.

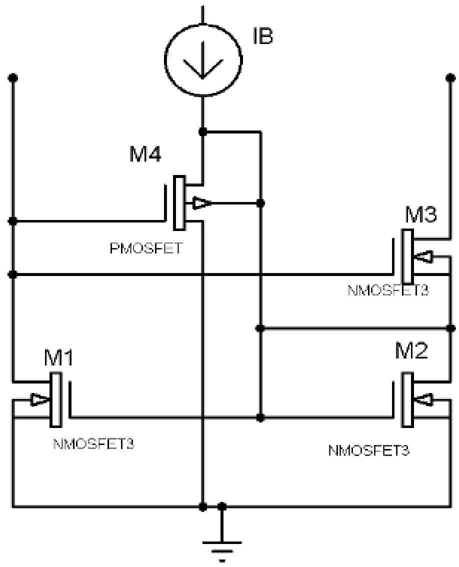

Figure 7

Level shifter technique has also been implemented for Cascode current mirrors[9], which usually require higher bias voltages to operate. However, the results obtained are much less significant than those of simple and Wilson mirrors in similar conditions.

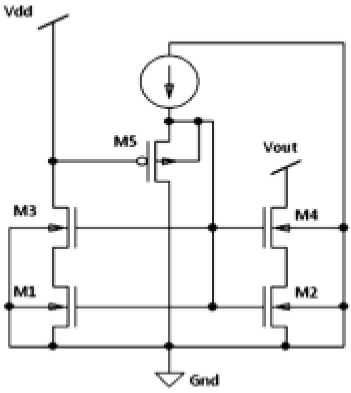

Figure 8

III. Simulation results

The results of Spice simulations are shown in charts in the following page. The Wilson current mirror in Fig. 2 has a 3dB cutoff frequency of about 762MHz, as can be seen from Chart 1. With the addition of active load compensation of this paper, the 3dB cutoff frequency for the modified Wilson mirror crosses 784MHz, i.e. an improvement of 22MHz, given in Chart 2.

Chart 3 shows improvement caused by just doubling the value of g_m in the MOSFET model. The cutoff frequency is now a little over 794MHz, resulting in a net improvement of about 32MHz. More bandwidth can yet be obtained by using still higher values of gm, as is shown in Chart 4.

The results of applying the level shifter configuration to the two versions of Wilson current mirror presented earlier are shown in charts 5 and 6. The use of level-shifting configuration facilitated precise current mirroring operation even at very low biasing voltages (2V). Thus, the voltage and power requirements of the analog IC get reduced by a great extent. It is noteworthy that the mirroring precision remains acceptable only for lower values of current, and it is poorer in the modified Wilson current mirror.

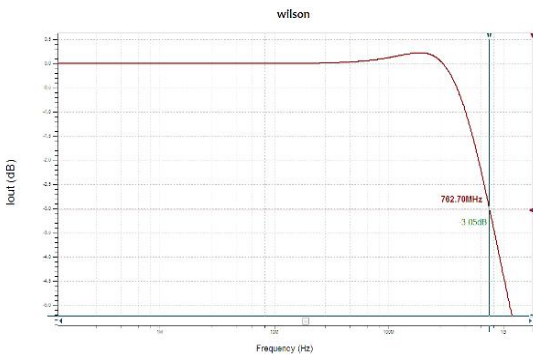

Chart 1: Frequency response of Wilson current mirror

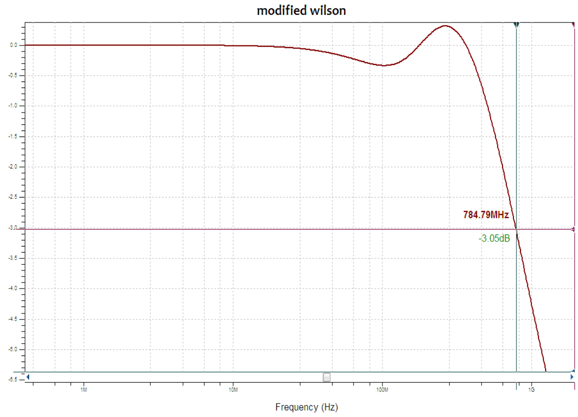

Chart 2: Response with active compensation

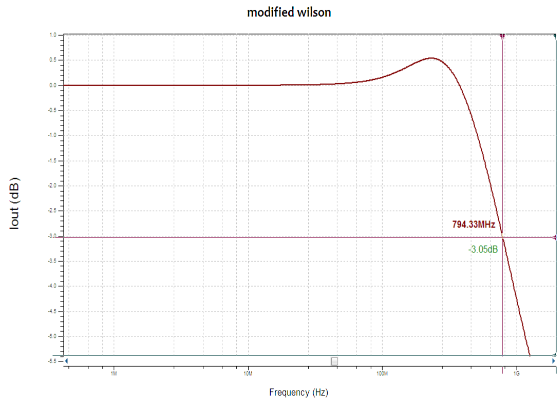

Chart 3: Response using twice the w/l ratio in active compensation

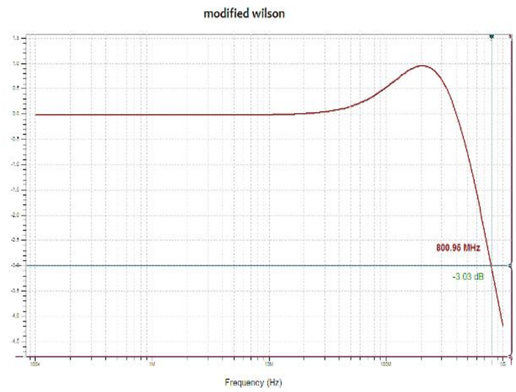

Chart 4: Response by increasing the w/l ratio by 4 times.

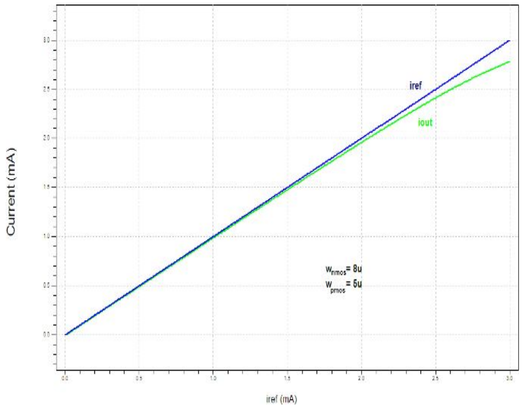

Chart 5: DC mirroring characteristics of level-shifted Wilson mirror of Fig. 7

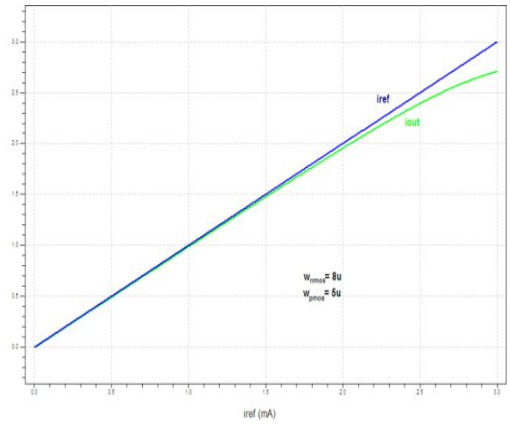

Chart 6: DC mirroring characteristics of modified Wilson mirror of Fig. 5 with level shifter applied to it

Table: Comparative results for different current mirror topologies.

Current Mirror	without resistance		with passive resistance		with active resistance	
	Bandwidth MHz	Power Dissipation mW	Bandwidth MHz	Power Dissipation mW	Bandwidth MHz	Power Dissipation mW
Simple Current Mirror	210.2	1.16	270.5	1.2	292.4	1.11
Wilson Current Mirror	762.70	4.1	784.79	4.7	794.33	4.5
Cascode Current Mirror	450	4.52	562	4.9	562	4.6
Level Shifted Wilson Mirror	762.70	1.2	784.79	1.5	794.33	1.7

IV. Conclusion

An improvement in the form of a compensation resistor between the gate terminals of two MOSFETs in the conventional Wilson current mirror has been proposed and studied. Both active and passive realization of the resistor has been considered. The active resistor is known to be easier to fabricate with a precisely controllable value, and offers potential for more bandwidth.

Likewise, low voltage operation of the current mirrors has been achieved by the use of level shifter technique in all the configurations. The biasing voltage requirement reduces to a good extent by the use of another p-MOS transistor which provides the required gate voltage to the primary transistors to achieve mirroring action. However, the use of level-shifter technique is subjected to an important limitation- the required increase in aspect ratio of the n-MOS transistors to achieve greater precision.

Taken together, these findings support strong recommendations to the use of Wilson current mirror configurations in low voltage and higher bandwidth applications and open up new possibilities which may be further studied and improved upon.

References

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