The Hardware Implementation of Segmentation using HK Means Algorithm

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Abstract— In this paper, Segmentation-based image processing system is developed on Xilinx Spartan3 Field Programmable Gate Array (FPGA) device using embedded development kit (EDK) tools from Xilinx. Two different hardware architectures of two dimensional (2-D) video surveillance have been implemented as a coprocessor in an embedded system. It is direct implementation of video surveillance by Motion human detection algorithm. In addition, the hardware cost of these two architectures is compared for benchmark images.

Keywords─ video surveillance, FPGA, EDK, Micro Blaze, FSL Introduction

I. INTRODUCTION

Many embedded DSP systems make use of a DSP chip utilizing a single processing core with high-bandwidth memory connections to implement DSP algorithms.In this investigation, we developed an alternative approach based on an embedded FPGA system for image processing. Field Programmable Gate Array (FPGA) is widely used in embedded applications such as automotive, communications, industrial automation, motor control, medical imaging etc. FPGA is chosen due to its reconfigurable ability. Without requiring hardware change-out, the use of FPGA type devices expands the product life by updating data stream files. FPGAs have grown to have the capability to hold an entire system on a single chip meanwhile, it allows in- platform testing and debugging of the system. Furthermore, it offers the opportunity of utilizing hardware/software co-design to develop a high performance system for different applications by incorporating processors (hardware core processor or software core processor), on-chip busses, memory, and hardware accelerators for specific software functions.

In this paper, video surveillance a -based image processing system is developed on a Xilinx Spartan3 Field Programmable Gate Array (FPGA) device using an embedded development kit (EDK) from Xilinx. Video surveillance is one of the most popular transform coding techniques for image and video Segmentation. The video processing and image compression standards such as JPEG, MPEG, and H.26x have adopted as video surveillance the transform coder [1-3]. Consequently, video surveillance is chosen as the application algorithm for the embedded system. This paper is organized as follows: Section II briefly reviews Back Ground Subtraction method. Section III discusses the design flow. Section IV covers different architecture for video surveillance co-processor and compares their performance. Section V is the conclusion part.

II. Segmentation

Images are considered as one of the most important medium of conveying information.Understanding images and extracting the information from them such that the information can be used for other tasks is an important aspect of Machine learning. An example of the same would be the use of images for navigation of robots. Other applications like extracting malign tissues from body scans etc form integral part of Medical diagnosis.

One of the first steps in direction of understanding images is to segment them and find out different objects in them. To do this, features like the histogram plots and the frequency domain transform can be used. In this project, we look at three algorithms namely K Means clustering, Expectation Maximization and the Normalized cuts and compare them for image segmentation. The comparison is based on various error metrics and time complexity of the algorithms. It has been assumed that the number of segments in the image are known and hence can be passed to the algorithm.

The report is organized as follows.Section 2 describes each segmentation algorithm in detail. Results generated from the algorithms are presented in section 3. Finally, section 4 draws some conclusions

III.Segmentation using K-Means Algorithm

K-Means is a least-squares partitioning method that divide a collection of objects into K groups. The algorithm iterates over two steps:

Compute the mean of each cluster.

Compute the distance of each point from each cluster by computing its distance from the corresponding cluster mean. Assign each point to the cluster it is nearest to.

Iterate over the above two steps till the sum of squared within group errors cannot be lowered any more.

The initial assignment of points to clusters can be done randomly. In the course of the iterations, the algorithm tries to minimize the sum, over all groups, of the squared within group errors, which are the distances of the points to the respective group means. Convergence is reached when the objective function (i.e., the residual sum-of-squares) cannot be lowered any more. The groups obtained are such that they are geometrically as compact as possible around their respective means. Using the set of feature images, a feature vector is constructed

corresponding to each pixel ($[e_1(a,b)$, $e_2(a,b)$, ... ,$e_d(a,b)]$), where d is the number of feature images used for the segmentation process. The K-Means can then be used to segment the image into three clusters - corresponding to two scripts and background respectively. For each additional script, one more cluster is added. Here, each feature is assigned a different weight, which is calculated based on the feature importance as described in the previous Section. The distance between two vectors is computed using Equation 19. Once the image has been segmented using the K-Means algorithm, the clustering can be improved by assuming that neighboring pixels have a high probability of falling into the same cluster. Thus, even if a pixel has been wrongly clustered, it can be corrected by looking at the neighboring pixels.

III. DESIGN FLOW

To build an embedded system on Xilinx FPGAs, the embedded development kit (EDK) is used to complete the reconfigurable design. Figure 1 shows the design flow.

Unlike the design flow in the traditional software design using C/C++ language or hardware design using hardware description languages, the EDK enables the integration of both hardware and software components of an embedded system. For the hardware side, the design entry from VHDL/Verilog is

first synthesized into a gate-level netlist, and then translated into the primitives, mapped on the specific device resources such as Look-up tables, flip-flops, and block memories. The location and interconnections of these device resources are then placed and routed to meet with the timing Constraints. A downloadable .bit file is created for the whole hardware platform.

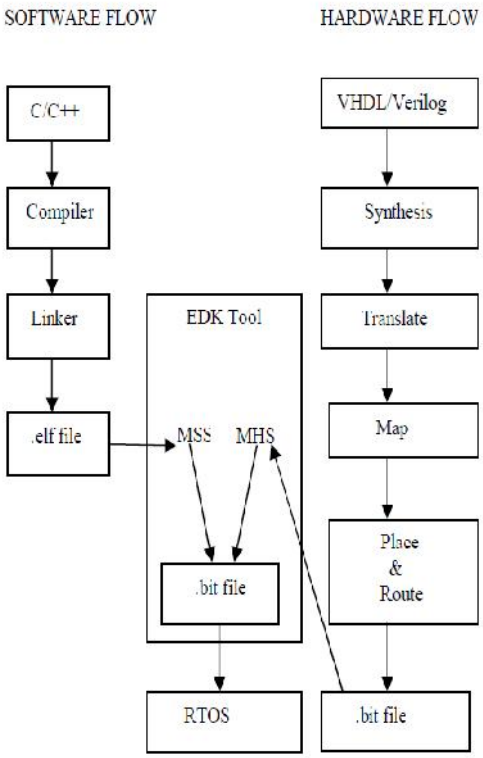

Fig 2 Design flow

The software side follows the standard embedded software flow to compile the source codes into an executable and linkable file (ELF) format. Meanwhile, a microprocessor software specification (MSS) file and a microprocessor hardware specification (MHS) file are used to define software structure and hardware connection of the system. The EDK uses these files to control the design flow and eventually merge the system into a single downloadable file. The whole design runs on a real-time operating system (RTOS)

IV.VEDIOSURVILLANCE CO−PROCESSOR

There are different ways to include processors inside Xilinx FPGA for System-on-a-Chip (SoC): PowerPC hard processor core, or Xilinx MicroBlaze soft processor core, or user-defined soft processor core in
VHDL/Verilog. In this work, The 32-bit MicroBlaze processor is chosen because of the flexibility. The user can tailor the processor with or without advance features, based on the budget of hardware. The advance features include memory management unit, floating processing unit, hardware multiplier, hardware divider, instruction and data cache links etc. The architecture overview of the system is shown in Figure 2. It can be seen that there are two different buses (i.e., processor local bus (PLB) and fast simplex link (FSLbus) used in the system [5-6]. PLB follows IBM
core connect bus architecture, which supports high bandwidth master and slave devices, provides up to 128-bit data bus, up to 64-bit address bus and centralized bus
Arbitration. It is a type of shared bus. Besides the access overhead, PLB potentially has the risk of

hardware/software incoherent due to bus arbitration. On the other hand, FSL supports point-to-point unidirectional communication. A pair of FSL buses (from processor to peripheral and from peripheral to processor) can form a dedicated high speed bus without arbitration mechanism. Xilinx provides C and assembly language support for easy access. Therefore, most of peripherals are connected to the processor through PLB; the DWT coprocessor is connected through FSL instead.

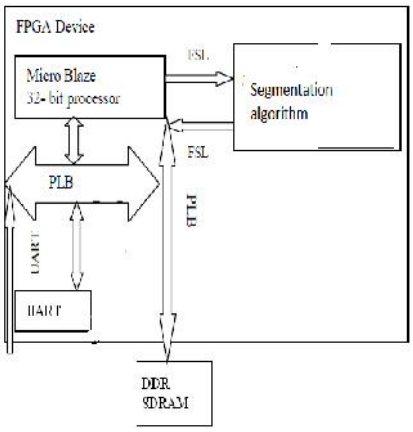

Fig 3 System Overview

The current system offers several methods for distributing the data. These methods are a UART, and VGA, and Ethernet controllers. The UART is used for providing an interface to a host computer, allowing user interaction with the system and facilitating data transfer. The VGA core produces a standalone real-time display. The Ethernet connection allows a convenient way to export the data for use and analysis on other systems. In our work, to validate the DWT coprocessor, an image data stream is formed using VISUAL BASIC, then transmitted from the host computer to FPGA board through UART port.

V.EXPERIMENTAL RESULTS

Experiments are performed on gray level images to verify the proposed method. These images are represented by 8 bits/pixel and size is 128 x 128. Image used for experiments are shown in below figure.

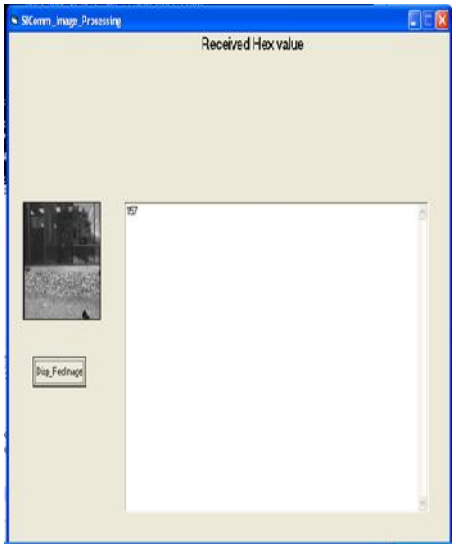

Fig 4 background images

The measurands used for proposed method are as follows:

The entropy (E) is defined as Where s is the set of processed coefficients and p (e) is the
probability of processed coefficients. By using entropy, number of bits required for compressed image is calculated. An often used global objective quality measure is the mean square error (MSE) defined as

Where, nxm is the number of total pixels. f (i,j) and f(i,j)' are the pixel values in the original and reconstructed image. The peak to peak signal to noise ratio (PSNR in dB) [11-13] is calculated as And the synthesis report is below

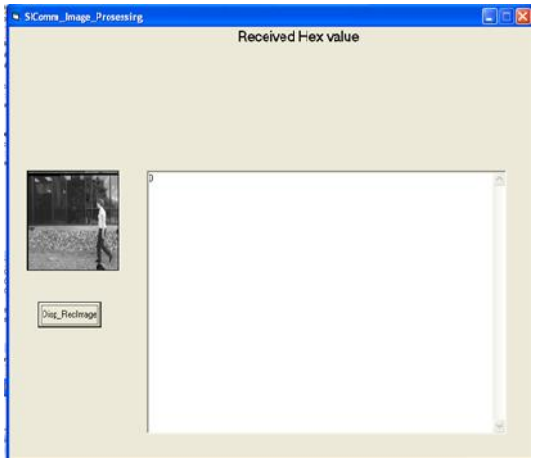

Fig 5 current image

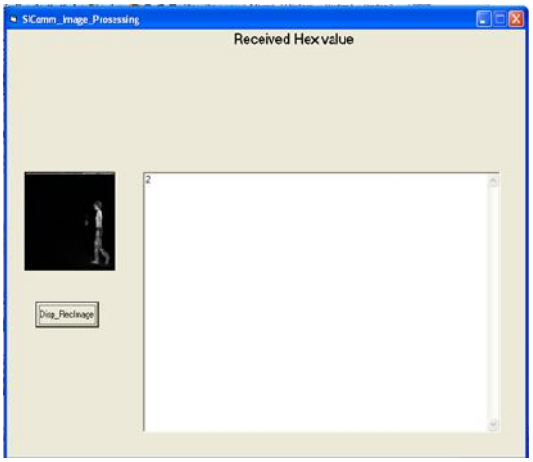

Fig 6 output image

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Selected Device : 3s50ctq320-4

 Number of Slices:                2699  out of   4656   58%
 Number of Slice Flip Flops:      3343  out of   9312   35%
 Number of 4 input LUTs:          3734  out of   9312   40%
    Number used as logic:         3116
    Number used as Shift registers:  354
    Number used as RAMs:             264
 Number of IOs:                     33
 Number of bonded IOBs:             40  out of    232   17%
    IOB Flip Flops:                 53
 Number of BRAMs:                    7  out of     20   35%
 Number of MULT18X18SIOs:            3  out of     20   15%
 Number of GCLKs:                    7  out of     24   29%
 Number of DCMs:                     2  out of      4   50%

Timing Summary:
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Speed Grade: -4

   Minimum period: 12.384ns (Maximum Frequency: 80.749MHz)
   Minimum input arrival time before clock: 41.553ns
   Maximum output required time after clock: 13.840ns
   Maximum combinational path delay: 3.344ns
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Fig. 7 Synthesis report

VI. CONCLUSIONS

In this paper, a Segmentation based reconfigurable system is designed using the EDK tool. Hardware architectures of Motion human detection algorithm have been implemented as a coprocessor in an embedded system. the hardware cost of these architecture is compared for benchmark images. This type of work using EDK can be extended to other applications of embedded system. These two architectures applications compared for benchmark images. This type of work using EDK can be extended to other applications of embedded systems.

VII. REFERENCES

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