Phase Noise repression in Fractional-N PLLs using Glitch-Free Phase Switching Multi-Modulus Frequency Divider

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Abstract— A novel programmable frequency divider for quantization noise (QN) suppression in fractional-N phase- locked loops (PLLs) is presented in this paper. The anticipated phase switching multi-modulus frequency divider (PS-MMFD) utilizes a novel Glitch-free phase switching (PS) divide-by-0.5/1/1.5/2 cell to reduce the rate of recurrence division step to 0.5 and its QN induced by modulation is thus suppressed by supplementary 6 dB. Contrast with other frequency dividers used for QN suppression, the future Glitch-free PS-MMFD is more robust, can operate at higher input frequency and devour less power. Detailed analysis and implementation of the proposed glitch-free PS-MMFD is established, followed by tentative results from a fully integrated \( \Delta \Sigma \) fractional-N PLL utilizing the proposed QN suppression technique. Implemented in a 0.18\( \mu \)m CMOS procedure, the projected glitch-free PS-MMFD occupies an area of 0.38 mm \( \times \)0.25 mm and consumes 5m\( A\) on or after a 1.8-V supply at an input frequency of 2 GHz. Measurement results also demonstrate the additional 6-dB QN suppression by the proposed technique.

I. INTRODUCTION

The \( \Delta \Sigma \) fractional-N phase-locked loop (PLL) is widely used in wireless communication systems, allowing tradeoffs among PLL design constrains for phase noise, settling time, frequency resolution, and reference spur. The modulator generates a pseudo-random bit sequence to dither the instantaneous division ratio and its time-average value equals to the required fractional division ratio. However, since the internal step of the frequency divider still remains discrete, the quantization error, i.e., the deviation from the desired fractional division ratio, introduces the quantization noise (QN) and deteriorates the overall phase noise performance especially for wideband PLLs. Several researchers used digital-to-analog converter (DAC) controlled current branches to compensate for the QN. The performance is mainly limited by the mismatch from DAC digital value to its analog counterpart. Many recent publications have been progressively improving the mismatch. Different kinds of adaptive algorithms are adopted, and the circuit implementations become dramatically complex.

A noise shaping technique is introduced in [7]. The groups of phase frequency detector (PFD) and charge pump (CP) combinations are controlled in such a way that the QN is equivalently filtered out by a digital finite-impulse response (FIR) filter. Another noise filtering technique [8] based on an integer- PLL in a feedback path suppresses out-of-band quantization noise of a high-order modulator. Nonetheless, both improvements of output phase noise are obtained at the cost of circuit complexity. Hybrid PFD/DAC structure was utilized in [9] to manipulate the PLL feedback signal and perform the equivalent QN compensation. However, such technique demands extremely high accuracy in timing control.

The most straightforward way to suppress the QN is to decrease the quantization step that is the internal division step in fractional- PLLs. There are several publications elaborating on this idea [10]–[12]. The QN is suppressed by 6 dB if reducing the division step by half. The key principle is to trigger the frequency divider on either rising or falling edges of the input signal to perform the double edge triggering [10], [11]. However, the robustness of the frequency divider cannot be guaranteed at high input frequencies because the operating frequency is actually twice of the input signal frequency. Our simulation results show the maximum input signal frequency of the divider introduced in [10] is limited to about 3.0 GHz in a 0.18 m CMOS process. In addition, the circuit stage performing the double edge triggering consumes more than half of the total power of the frequency divider. The above shortcomings of the double edge triggering technique restrict its use in the low-power high-frequency applications.

In this paper, a novel circuit technique, glitch-free phase switching multi-modulus frequency divider (PS-MMFD) to suppress the QN in a fractional- PLL, is proposed [12]. The division step of the PS-MMFD is 0.5, and its QN induced by modulation is thus suppressed by additional 6 dB. In addition, the PS-MMFD could operate at a higher frequency since its internal operating frequency is not doubled. Furthermore, a wide continuous frequency division range is achieved in the proposed PS-MMFD by using division ratio extension logic. A fractional- PLL utilizing the proposed glitch-free PS-MMFD is also designed and implemented in a 0.18 m CMOS process to demonstrate its performance.

Fig.1. Phase noise profile with and without QN suppression

The contents of this paper are organized as follows. Section II illustrates the concept of the QN suppression technique and two state-of-the-art programmable frequency dividers for QN suppression. Section III describes the detailed architecture and circuit implementation of the proposed glitch-free PS-MMFD. Practical design considerations are also discussed in this section. Simulation results and measurement results are presented in Section IV, followed by the conclusions in Section V.

II. QUANTIZATION NOISE SUPPRESSION

A. Quantization Noise

The QN-induced phase noise degradation at the output of the PLL can be expressed as

\[ S_{\Delta x}(f) = f_{\text{REF}} \cdot |H_{\Delta x}(o/f_{\text{REF}})|^2 \cdot \left( |T_{\text{DIV}}(o/2f_{\text{REF}}, jf)|^2 \cdot \frac{\Delta^2}{12} \right) \tag{1} \]

where \( f_{\text{REF}} \) is the reference frequency of the PLL; \( H_{\Delta x}(Z) \) is the QN transfer function of \( \Delta x \) modulation, which depends on the structure of the \( \Delta x \) modulator; \( T_{\text{DIV}}(Z,jf) \) is the transfer function from the divider output to the PLL output; \( \Delta \) is the step of the quantization (usually \( \Delta = 1 \) for integer step frequency divider); and \( S_{\Delta x}(jf) \) is the power spectrum density of QN-induced PLL output phase noise.

The QN introduced by the deviation of instantaneous division ratio and desired fractional division ratio is high-pass filtered by the modulation, while the noise transfer function from the divider output to the PLL output demonstrates low-pass characteristic. Thus, the total QN-induced phase noise degradation presents a little hump in the PLL output phase noise as shown in Fig. 1 (the dash and dash-dotted lines).

An ultra-high-frequency (UHF) band digital TV tuner application is used here as an example to show the necessity of the QN suppression. The phase noise mask required for a typical UHF digital TV tuner is shown in Fig. 1 (the solid line). As can be seen, if the QN-induced phase noise degradation is not fully suppressed, the little hump could be visible in the overall PLL output phase noise curve at high offset frequency, and the phase noise performance would fail to fit into the derived TV tuner phase noise mask requirements.

B. Programmable Frequency Dividers For QN Suppression

The pulse-swallow frequency divider and the truly modular frequency divider [22], [23] are widely used in PLLs for wireless communication systems and both of them have already been extended for QN suppression.

1) Pulse-Swallow Frequency Divider for QN Suppression:

Different from the traditional architectures [16], pulse-swallow frequency divider with QN suppression adopts dual-modulus prescaler with step size of 0.5 instead of 1 as shown in Fig. 2 [11]. The dual-modulus prescaler divides the input frequency either by or according to the modulus control signal, mod. The total division ratio of the pulse-swallow frequency divider for QN suppression can be expressed as follows:

\[ N_{\text{div}} = S \times (N+0.5) + (P-S) \times N = N \times P + 0.5 \times S \tag{2} \]
Truly modular frequency divider with QN suppression

In order to get the continuous division ratio, the value of is limited to; meanwhile, should be guaranteed. Therefore, the minimum division ratio of this kind of pulse-swallow programmable divider is and its maximum division ratio is , where is the maximum division ratio of the program counter.

One possible realization of such dual-modulus prescalers, a divide-by-4/4.5 (4/4.5) topology, is also shown in Fig. 2 [11]. Compared with conventional divide-by-4/5 (4/5) prescaler, the 4/4.5 divider cell is composed of four D-flip-flops (DFFs), two multiplexers (MUXs) and two D-latches which are all synchronized at the highest input frequency [11], among which D-latch1, D-latch2, and MUX2 form a double-edge-triggered flip-flop (DTFF) (shown in Fig. 2) [24], and each DFF is composed of a positive D-latch and a negative D-latch. When mod is high, the DTFF is enabled, and generates a signal which lags half input cycle of selected DFF output. The signal feedbacks to DFFs input and a half input cycle is swallowed due to its delay.

Two issues limit the use of this divider in PLLs for wideband wireless communication systems. First, the minimum continuous division ratio is twice as that of divide-by prescaler, which may be not suitable for high reference frequency applications; Second, the power consumption is high because of the extra DFF, MUX, and DTFF for extending division ratio step to 0.5, while the conventional /4/5 prescaler contains only 3 DFFs (6 D-latches). The extra circuits are operating at the highest frequency with double-edge-triggered operation and the total power consumption is almost doubled.

2) Truly Modular Frequency Divider for QN Suppression: The general architecture of truly modular frequency divider with QN suppression composed of a divide-by-1/1.5 (1/1.5) divider cell [10], a traditional divide-by-2/3 (2/3) chain, and a few logic gates to extend the division ratio is shown in Fig. 3 [22]. The division ratio can be expressed as follows

\[ N = 2^{m} \cdot \prod_{k=0}^{m} \begin{cases} p_{k} & \text{if } k \pmod{2} = 0 \\ \bar{p}_{k} & \text{if } k \pmod{2} = 1 \end{cases} + 2^{m-2} \cdot p_{m-1} + \cdots + 2^{0} \cdot p_{1} + 2^{-1} \cdot p_{0} \]  

where \( m \) is the minimum effective length of the /2/3 chain, \( n \) is the total divider stages including a /1/1.5 divider cell and the /2/3 chain, and is the division ratio control word. The division ratio range is from \( 2^{m} \) to \( 2^{m-0.5} \).

The topology of the /1/1.5 divider cell added in front of the /2/3 chain is shown in Fig. 4 [10]. It is used to achieve QN suppression by reducing the division step to 0.5. The /1/1.5 divider cell consists of two arts, i.e., the prescaler logic and the end-of-cycle logic. When both mod and are high, it is in divide- by-1.5 mode, the prescaler logic swallows half input cycle due to the delay of end-of-cycle part; otherwise, the /1/1.5 divider cell tracks the input by the DFF composed of D-latch1 and D-latch2. The end-of-cycle part is based on a DTFF which inherently doubled the operating frequency of the divider.

Potential timing racing problem exists due to the relationship of the input-to-DFF delay (or input-to-latch delay) and input-to-MUX delay in divide-by-1.5 mode [10]. Furthermore, employing the /1/1.5 divider cell suppresses the QN induced phase noise but increases power consumption by about 20% and decreases the maximum operating frequency.

3) Summary: Both aforementioned programmable frequency dividers for the QN suppression are based on double-edge-triggering. Though it achieves a 0.5 division step, double-edge-triggering limits the highest input frequency of the frequency divider and demands larger power consumption because the frequency divider essentially operates at twice of the input frequency.

A phase-frequency detector is an asynchronous sequential logic circuit originally made of four flip-flops (i.e., the phase-frequency detectors found in both the RCA CD4046 and the motorola MC4344 ICs introduced in the 1970s). The logic determines which of the two signals has a zero-crossing earlier or more often. When used in a PLL application, lock can be achieved even when it is off frequency and is known as a Phase Frequency Detector. Such a detector has the advantage of producing an output even when the two signals being compared differ not only in phase but in frequency. A phase frequency detector prevents a "false lock" condition in PLL applications, in which the PLL synchronizes with the wrong phase of the input signal or with the wrong frequency (e.g., a harmonic of the input signal).

A bang-bang charge pump phase detector supplies current pulses with fixed total charge, either positive or
negative, to the capacitor acting as an integrator. A phase detector for a bang-bang charge pump must always have a dead band where the phases of inputs are close enough that the detector fires either both or neither of the charge pumps, for no total effect. Bang-bang phase detectors are simple, but are associated with significant minimum peak-to-peak jitter, because of drift within the dead band.

In 1976 it was shown that by using a three-state phase detector configuration (using only two flip-flops) instead of the original RCA/Motorola twelve-state configurations, this problem could be elegantly overcome. For other types of phase-frequency detectors other, though possibly less-elegant, solutions exist to the dead zone phenomenon.[3] Other solutions are necessary since the three-state phase-frequency detector does not work for certain applications involving randomized signal degradation, which can be found on the inputs to some signal regeneration systems (e.g., clock recovery designs).

A proportional phase detector employs a charge pump that supplies charge amounts in proportion to the phase error detected. Some have dead bands and some do not. Specifically, some designs produce both "up" and "down" control pulses even when the phase difference is zero. These pulses are small, nominally the same duration, and cause the charge pump to produce equal-charge positive and negative current pulses when the phase is perfectly matched. Phase detectors with this kind of control system don't exhibit a dead band and typically have lower minimum peak-to-peak jitter when used in PLLs. In PLL applications it is frequently required to know when the loop is out of lock. The more complex digital phase-frequency detectors usually have an output that allows a reliable indication of an out of lock condition. The phase detector generates the error signal required in the feedback loop of the synthesizer. The majority of PLL ASICs use a circuit called a Phase Frequency Detector (PFD) similar to the one shown in Figure. Compared with mixers or XOR gates, which can only resolve phase differences in the +/- p range, the PFD can resolve phase differences in the +/- 2p range or more (typically “frequency difference” is used to describe a phase difference of more than 2p, hence the term “phase frequency detector.” This circuit shortens transient switching times and performs the function in a simple and elegant digital circuit.

The PFD compares the reference signal Fr with that of the divided down VCO signal (Fvco/N) and activates the charge pumps based on the difference in phase between these two signals. The operational characteristics of the phase detector circuitry can be broken down into three modes: frequency detect, phase detect, and phase locked mode. When the phase difference is greater than ±2p, the device is considered to be in frequency detect mode. In frequency detect mode the output of the charge pump will be a constant current (sink or source, depending on which signal is higher in frequency.) The loop filter integrates this current and the result is a continuously changing control voltage applied to the VCO. The PFD will continue to operate in this mode until the phase error between the two input signals drops below 2p. Once the phase difference between the two signals is less than 2p, the PFD begins to operate in the phase detect mode. In phase detect mode the charge pump is only active for a portion of each phase detector cycle that is proportional to the phase difference between the two signals (see Figure). Once the phase difference between the two signals reaches zero, the device enters the phase locked state (see Figure.)

![Phase Frequency Detector](image)

In the phase locked state, the PFD output will be narrow “spikes” that occur at a frequency equal to Fr. These current spikes are due to the finite speed of the logic circuits (see Figure 8, DOA blowup) and will have to be filtered so they do not modulate the VCO and generate spurious signals.

### III. PHASE SWITCHING MULTI MODULUS FREQUENCY DIVIDER

A novel multi-modulus frequency divider based on a divide-by-0.5/1/1.5/2 (/0.5/1/1.5/2) cell utilizing glitch-free phase switching (PS) technique is proposed to improve the performance for the QN suppression. Compared with the techniques discussed in Section II, the proposed PS-MMFD is robust without any timing racing or glitch problems and...
achieves the desired 6 dB QN suppression while consuming less power and operating at higher input frequencies.

A. Unconditional Glitch-Free Phase Switching:

Fig. 7. Phase Switching (a) Glitch-Ocurred.(b) Glitch-Free

The basic idea of phase switching is first proposed in [17] as shown in Fig. 7(a). The high-frequency input directly feeds into a divide-by-2 quadrature phase generator and the four 90° phase apart outputs, are Grey-Coded as states (0°), (90°), (180°), and (270°).

When a PS is required, the output switches to the next state [e.g., from (180°) to (270°) as shown in Fig. 7(a)]. Compared with the waveform of no PS occurrence, the rising edges are moved backward by half of the input cycle as the solid arrows indicate in Fig. 7(a).

Fig. 8. Proposed glitch-free PS-MMFD architecture.

When the PS occurs at time, it operates properly. However, if the PS occurs a little earlier at, an unwanted narrow pulse is generated. Although the rising edges of the output are moved backward as normal, an additional rising edge would be counted because of the unwanted pulse (glitch). The phase information will be corrupted and the function of the overall frequency divider would be failed.

Glitches can be avoided by using long rising time control signals for output selecting multiplexer which is not a robust solution [17]. A retimer circuit can also be inserted between the quadrature phase generator and the multiplexer to synchronize the four outputs and the corresponding control signals before they feed into the multiplexer to eliminate the glitches [18]. However, this solution increases the circuit complexity.

The simplest solution for the undesirable glitch problem is shown in Fig. 7(b) [19], [20]. In this case, the rising edges are moved forward by half of the input cycle as the solid arrows indicate. Different from the backward movement, whether the PS occurs at or , the only difference is the duty cycle of current period, and such duty cycle variation will not influence the function of the frequency divider.

In summary, for unconditionally glitch-free PS between the current phase state and the next phase state, the next phase state has to be in its logic high when the rising edges of the current phase state occur. For example, the PS from (270°) to (180°) (as shown in Fig. 7) is glitch-free while it is not the case for the PS from (270°) to (90°). This is because the rising edges of (270°) see the logic high in (180°) but the transition moments in (90°). The PS from the current phase state to its corresponding lead-90 phase state, i.e., the nearest-reversed-state PS, is guaranteed to be glitch-free as shown in Fig. 7(b).

B. Proposed Glitch-Free PS-MMFD

The overall architecture of the proposed Phase Switching multi-modulus frequency divide (PS-MMFD) is shown in Fig. 6. It is mainly composed of a divide-by-
0.5/1/1.5/2 (/0.5/1/1.5/2) cell, several divide-by-2/3 (2/3) cells and the division range extension logic circuit.

The frequency division ratio, is controlled by the 10-bit division ratio control input, . With the division range extension logic, the division ratio of the proposed PS-MMFD can be expressed as follows:

\[
N = 2^5 \cdot \prod_{i=6}^{9} p_i + 2^3 \cdot p_0 + 2^1 \cdot p_3 + \cdots + 2^1 \cdot p_2 + 2^0 \cdot p_1 + 2^1 \cdot p_0.
\]

\[(4)\]

C. Divide-by-0.5/1/1.5/2 Cell

The operating principle of the divide-by-0.5/1/1.5/2 (/0.5/1/1.5/2) cell extends the basic glitch-free phase switching technique proposed in [19], [20]. It is composed of a divide-by-2 quadrature phase generator, a phase selector and a digital controller CTRL, as shown in Fig. 6. The divide-by-2 in /0.5/1/1.5/2 cell works at full speed, and generates four Grey-coded outputs whose rising edges (or phases) are separated by 90°. At any instance, only one of the divide-by-2 outputs is connected to the subsequent 2/3 chain through a 2-bit MUX. The MUX is controlled by the 2-bit word, given by the control circuit block (CTRL). In order to achieve the required four division ratios (/0.5/1/1.5/2), the CTRL logic for glitch-free PS has to be carefully designed.

To guarantee the operation of unconditionally glitch-free phase switching in /0.5/1/1.5/2 cell, the CTRL logic has to ensure that only nearest-reversed-state PS can be performed through the MUX. When one nearest-reversed-state PS is finished, the following rising edges of the /0.5/1/1.5/2 cell output phase state seem to be moved forward by one half input cycle compared to the original output phase state, effectively reducing the period of final divider output by half input cycle, i.e., divide-by- becomes divide-by- as depicted in Fig. 7. In order to obtain the continuous division ratio stepped by 0.5, the phase switching module should be able to conduct 0-3 times of nearest-reversed-state PS in an output cycle to realize the divide-by-/0.5/1/1.5/2.

Fig. 7. Timing diagram of one phase switching.

Fig. 8 shows the detailed implementation of the CTRL circuit block. The CTRL is mainly composed of a pulse generator, a grey-coded finite state machine (FSM), a 2-bit counter and some logic control circuits (compare logic). The topology of the pulse generator is shown in Fig. 9(a) [25]. The data input of the positive latch is always connected to logic high. For each falling edge of the clock signal, the output follows the input to transfer to logic high if rst signal is disabled. However, the output is also served as the rst signal through a delay cell which will set the output to logic low. The transient waveforms of the pulse generator are shown in Fig. 9(b). As can be seen from Fig. 9(b), a short pulse rst b is generated to reset the 2-bit counter to state at each falling edge of the PS-MMFD output, fout. The digital clock, clk dig, passing through a buffer, synchronizes the FSM and the 2-bit counter by its falling edges. The state transition graphs of the FSM and the 2-bit counter are shown in Fig. 10(a) and (b), respectively.

Fig. 8. CTRL circuit block.
The input, which gives the total number of required glitch-free nearest-reversed-state PS steps in current output cycle, is synchronized by the falling edges of the PS-MMFD output before it is compared with the number of finished glitch-free nearest-reversed-state PS steps in the compare logic (CL) circuit block. The CL output, en, which controls the operating state of the FSM and the 2-bit counter, will remain valid before all required glitch-free nearest-reversed-state PS steps finished. The output of the CTRL, i.e., the output of the FSM, gives the 2-bit MUX control word to control the switching among the four phase states (shown in Fig. 8).

### D. Circuit Implementation of PS-MMFD

The PS-MMFD is mainly composed of a /0.5/1/1.5/2 cell and a /2/3 chain. The /2/3 chain in the proposed PS-MMFD is composed of the truly modular dividers shown in Fig. 12 [22]. The key principle of /2/3 cell is to swallow one additional input cycle when the input control and the feedback signal are valid. The input frequencies are stepped down through the divider chain, so the power consumption can be scaled down progressively.

The basic logic cells used in the PS-MMFD are mainly D-latches, AND-gated D-latches, and MUXs. The implementation of these logic cells includes CMOS static logic [25], true single-phase clock-based (TSPC) logic [26], [27], differential cascode voltage-switch-logic (DCVSL) [28], and current mode logic (CML) [29], [30]. Their usage varies according to their application and input signal frequency. As regards to the high-speed frequency divider design, CML is most commonly used for its robustness and noise performance at a cost of a little higher power consumption. In the proposed PS-MMFD, all the blocks above the dashed line shown in Fig. 6 are CML circuits except the CML-to-CMOS converter and the CTRL block in /0.5/1/1.5/2 cell. CMOS static logic is adopted in the other blocks.

The circuit implementation of the CML AND-gated D-latch is shown in Fig. 12. The size of the load resistor, the tail current source, and the width of each differential pair including the clock inputs, the signal inputs, and the cross-coupled pair, are all carefully designed according to the operating frequency, the required output swing and load capacitance for power consumption optimization [29].

Furthermore, degeneration resistors are used to improve the noise performance of the CML latches especially the flicker noise.
noise of the transistors and in the tail current source. The degeneration resistance is inversely proportional to the current in the branch to maintain same dc voltage at the sources. The output flick noise at node (shown in Fig. 12) is demonstrated in (5) and (6) respectively:

\[
\frac{\bar{v}_{\text{in},1/f,M1}^2}{\bar{v}_{\text{out},1/f,M1}^2} = \left( \frac{k}{1 + g_m R} \right)^2
\]

\[
\frac{\bar{v}_{\text{in},1/f,M2}^2}{\bar{v}_{\text{out},1/f,M2}^2} = \left( \frac{1}{1 + g_m R} \right)^2
\]

where \(\bar{v}_{\text{in},1/f,M1}\) is the flick noise of \(M1\), \(\bar{v}_{\text{in},1/f,M2}\) is the flick noise of \(M2\), \(k\) is the current-mirror gain, and \(g_m\) is the transconductance of \(M1\). It is obvious that the flick noise of both transistors is decreasing by the ratio of \((1 + g_m R)^2\). The thermal noise introduced by the degeneration resistor is negligible compared with the transistor flick noise.

The phase noise optimization for CML /2/3 cell with the degeneration resistor is also verified in simulation as shown in Fig. 13. The phase noise is 4.9 dB better at 1-kHz frequency offset because the low-frequency dominant flick noise is suppressed by the degeneration resistor. The effect is not so obvious at high offset frequency, only about 1.8 dB better at 10-MHz offset, where the load resistor noise is dominant and the thermal noise contribution from the degeneration resistors is increased.

The digital latches adopted in CMOS static /2/3 cells are negative and positive latches based on MUXs [25]. The digital /2/3 cell is reusable, therefore facilitating the circuit design. The CML-to-CMOS block is composed of a conventional differential-to-single-ended opamp and an inverter chain. The division ratio extension logic is composed of CMOS logic cells, e.g., NAND-gates, NOR-gates, and inverters.

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**E. Practical Timing Issues**

The falling edge of the PS-MMFD output starts a new output cycle and it is necessary to schedule the PS of /0.5/1/1.5/2 cell and the swallows in /2/3 chain properly to perform the desired frequency division. Three practical timing issues which might corrupt the function of the PS-MMFD are discussed as follows.

1) **Setup Time of FSM and Counter:** As shown in Figs. 5, 8, and 14, the falling edge of clk dig serves as the clock signal for the FSM and counter in CTRL circuit block. Ideally, the setup time for the FSM and the counter is about 6 input cycles; however, considering the pulse width variation of rst_b (shown in Figs. 8, 9, and 14) and the propagation delay of clk dig, additional delay (clk buf shown in Fig. 8) for clk dig is inserted to guarantee enough setup time for the FSM and the counter in CTRL.

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**Fig. 12. CML AND-gated D latch**

**Fig. 13. Simulated phase noise performance of CML /2/3 cell with and without degeneration R.**
2) **Division Ratio Control Inputs Timing:** For fractional-PLLs, the division ratio will change in every cycle. The division ratio control inputs, could all be clocked by the falling edges of output. However, due to the propagation delay and process variations, the feedback signals of /2/3 cells, i.e., might be generated during the transition of their corresponding control inputs, which creates uncertainty. To avoid this, the division ratio control inputs of /0.5/1.5/2 cell are clocked by the falling edges of but the division ratio control inputs for /2/3 cells are clocked by the rising edges of to ensure that always sees a stable control input.

3) **Phase Switching Timing:** For any instantaneous division ratio, all the required nearest-reversed-state PS steps need to be accomplished within current output cycle to achieve the immediate division ratio changing, which is crucial to the function of fractional-PLLs. As can be seen from Fig. 6, the output is the feedback signal of the CMOS static /2/3 cell chain, and the above requirement can be interpreted as all the nearest-reversed-state PS steps should be finished before the first two feedback signals, and , are ready to swallow one cycle for the next division period (shown as the shaded region in Fig. 14). A digital signal which can afford at least three effective edges in an output cycle s needed to clock the CTRL circuit block.

In the most critical case that only five stages of /2/3 cells are enabled, theoretically either double-edge triggered clock, clk_dig_old, or falling-edge triggered clock, clk_dig, could be used as the clock signal for the FSM and the counter. Fig. 14 shows the ideal waveform in the most stringent case for both setup time and PS timing issues.

In this case, three nearest-reversed-state PS steps are required in one output cycle. It is clear that the PS timing margin is about 16 input cycles if clk_dig is used compared with potentially insufficient 8 input cycles if clk_dig_old is used (shown in Fig. 14). Considering the propagation delay and the intentionally added delay, the third nearest-reversed-state PS step might fall out of the shaded region if double-edge triggered clk_dig_old was adopted as the clock signal. Therefore, the most efficient clock signal for the FSM and the counter has to be clk_dig.
Fig. 16. PLL prototype with the proposed PS-MMFD.

Relevant circuit simulation results are shown in Fig. 15 for the most stringent case at the highest input frequency. Compared with the behavior simulation waveforms in Fig. 15, the supposed aligned edges deviate from their ideal places quite a lot (noted by arrows in Fig. 15) due to practical circuit limitations. However, all the PS-MMFD functionality is preserved, and both the setup time and PS timing margin are still quite sufficient because of the proper timing control methods discussed before.

As a side note, for division ratio, the PS timing margin might be potentially insufficient at high input frequencies even clk_dig is used as the clock. Since these division ratios are usually useless in real applications, they can be simply abandoned for robust PS-MMFD performance.

IV. EXPERIMENTAL RESULTS

A Δ∑ fractional-N PLL utilizing the proposed glitch-free PS-MMFD is designed and implemented in a 0.18µm CMOS process to demonstrate the performance of PS-MMFD. Fig. 16 shows the block diagram of the implemented PLL. Conventional tri-state PFD [16] is used to drive a current steering CP [31]. A cross-coupled dual-core VCO assisted with an efficient auto frequency calibration (AFC) [32] achieves a wide tuning range. The PS-MMFD together with the single loop modulator [13] is employed to generate feedback signal for the PFD. The PLL is fully integrated with an on-chip third-order loop filter.

Simulation results show that given an 8-mA total current consumption, the maximum input frequency of the PS-MMFD is about 3.8 GHz and the robust continuous division ratio is from 38.5 to 510 at the maximum input frequency across all process, voltage supply, and temperature (PVT) variations [12]. In measurements, we set the input frequency to about 2 GHz since the available maximum VCO frequency is about 2 GHz. The 3-bit Δ∑ modulator switching the division ratio for next f_{out} cycle from current state is limited to three steps upwards or four steps downwards. Simulation results of division ratio switching at 2-GHz input frequency across all PVT variations are shown in Fig. 17. The division ratio changes from 34.5 to 37.5 with as its original state as required.

Fig.17.simulated division ratio switching in PS-MMFD from N=36.5f_{in}=2.0GHz

![Fig.17.simulated division ratio switching in PS-MMFD from N=36.5f_{in}=2.0GHz](image)

Fig.18. PS-MMFD outputs. (a) PLL is locked. (b) N=30.5-32. (c)N=36.5-38.5.

The PS-MMFD is measured under various conditions with a 26-MHz signal as the reference clock. Fig. 18(a) is the measurement result of PS-MMFD outputs when the PLL is locked. Fig. 18(b) and (c) illustrates the PS-MMFD outputs with different division ratios when the input frequency is set to about 2 GHz. The PS-MMFD output waveforms together with
the input signal when varies from 30.5 to 32 are shown in Fig. 18(b). It is clearly seen that the required division ratios and continuous division ratios with a step size of 0.5 are realized. The PS-MMFD output waveforms when N varies from 36.5 to 38.5, which are the most stringent cases for PS timing, are shown in Fig. 18(c).

The PLL output phase noise is measured at different carrier frequencies of 950, 1315, and 1730 MHz, respectively, as shown in Fig. 19. The fractional-

\[ N \]

PLL is configured to different quantization levels of 0.5, 1, and 2 to show the performance difference. With a quantization level of 0.5, the PS-MMFD operates as proposed. With a quantization level of 1, the /0.5/1/1.5/2 cell operates as a /1/2 dual-modulus prescaler. With a quantization level of 2, the /0.5/1/1.5/2 cell operates as a divide-by-2 cell. It can be seen from Fig. 21 that the out-of-band phase noise contributed by the modulator is reduced with the help of the proposed half stepped PS-MMFD quantization level. Not surprisingly, the in-band phase noise for step size of 0.5 is also better than that for step size of 1 or 2 because the nonlinear behavior of PFD and CP is less severe and less QN at high offset frequencies is folded back [33]. The measurement results for the PLL out-of-band phase noise together with the corresponding VCO phase noise are summarized in Table I.

**TABLE I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>500kHz</th>
<th>1MHz</th>
<th>1.5MHz</th>
<th>2MHz</th>
<th>3MHz</th>
<th>4MHz</th>
<th>6MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Noise (dBc/Hz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCO</td>
<td>-126.5</td>
<td>-132.6</td>
<td>-135.8</td>
<td>-136.1</td>
<td>-136.5</td>
<td>-141.8</td>
<td>-143.9</td>
</tr>
<tr>
<td>( \Delta = 0.5 )</td>
<td>-125.6</td>
<td>-132.1</td>
<td>-134.3</td>
<td>-134.8</td>
<td>-136.5</td>
<td>-137.4</td>
<td>-141.2</td>
</tr>
<tr>
<td>( \Delta = 1 )</td>
<td>-123.1</td>
<td>-129.4</td>
<td>-130.6</td>
<td>-131.2</td>
<td>-132.7</td>
<td>-136.3</td>
<td>-137.7</td>
</tr>
<tr>
<td>( \Delta = 2 )</td>
<td>-122.0</td>
<td>-125.8</td>
<td>-125.8</td>
<td>-126.4</td>
<td>-127.1</td>
<td>-131.2</td>
<td>-134.8</td>
</tr>
<tr>
<td>( f_{\text{ref}} = 133.5 \text{MHz} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCO</td>
<td>-122.3</td>
<td>-129.7</td>
<td>-133.8</td>
<td>-135.6</td>
<td>-139.2</td>
<td>-141.5</td>
<td>-143.9</td>
</tr>
<tr>
<td>( \Delta = 0.5 )</td>
<td>-122.3</td>
<td>-135.7</td>
<td>-131.9</td>
<td>-133.8</td>
<td>-136.7</td>
<td>-139.6</td>
<td>-143.7</td>
</tr>
<tr>
<td>( \Delta = 1 )</td>
<td>-121.3</td>
<td>-137.2</td>
<td>-129.3</td>
<td>-130.3</td>
<td>-133.1</td>
<td>-135.7</td>
<td>-142.6</td>
</tr>
<tr>
<td>( \Delta = 2 )</td>
<td>-120.2</td>
<td>-123.5</td>
<td>-124.8</td>
<td>-125.2</td>
<td>-126.2</td>
<td>-130.2</td>
<td>-140.0</td>
</tr>
<tr>
<td>( f_{\text{ref}} = 180 \text{MHz} )</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>VCO</td>
<td>-121</td>
<td>-127.4</td>
<td>-130.8</td>
<td>-133.5</td>
<td>-137.2</td>
<td>-139.4</td>
<td>-142.6</td>
</tr>
<tr>
<td>( \Delta = 0.5 )</td>
<td>-118.4</td>
<td>-125.7</td>
<td>-128.6</td>
<td>-130.7</td>
<td>-134.1</td>
<td>-135.7</td>
<td>-138.9</td>
</tr>
<tr>
<td>( \Delta = 1 )</td>
<td>-119.5</td>
<td>-125.8</td>
<td>-126.4</td>
<td>-129.5</td>
<td>-131.4</td>
<td>-134.6</td>
<td>-138.6</td>
</tr>
<tr>
<td>( \Delta = 2 )</td>
<td>-116.4</td>
<td>-123.8</td>
<td>-124.3</td>
<td>-126.8</td>
<td>-129.6</td>
<td>-132.9</td>
<td>-134.1</td>
</tr>
</tbody>
</table>

**TABLE II**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18\mu\text{m CMOS}</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>5\text{mA}+1.8 \text{V (at 1.575 GHz)}</td>
</tr>
<tr>
<td>Division Ratio</td>
<td>20.5-90X</td>
</tr>
<tr>
<td>Operating Frequency Range</td>
<td>0.9-2.8 GHz</td>
</tr>
<tr>
<td>Synthesizer Phase Noise</td>
<td>-94dBc/Hz</td>
</tr>
<tr>
<td>Chip Size</td>
<td>2.1\text{mm}x0.92\text{mm (whole PLL)}</td>
</tr>
<tr>
<td>Power</td>
<td>0.5\text{mW}+0.25\text{mW (PS-MMFD)}</td>
</tr>
</tbody>
</table>

*Due to limited VCO frequency, the minimum operating frequency of 3.5 GHz is simulation result.

**TABLE III**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Size</td>
<td>2.1\text{mm}x0.92\text{mm (whole PLL)}</td>
</tr>
<tr>
<td>Power</td>
<td>0.5\text{mW}+0.25\text{mW (PS-MMFD)}</td>
</tr>
</tbody>
</table>

The PLL output phase noise is measured at different carrier frequencies of 950, 1315, and 1730 MHz, respectively, as shown in Fig. 19.
Compared with the case where the quantization level equals 1, the output phase noise suppression achieves maximum values of 5.8, 4.6, and 2.7 dB, respectively, at about 3-MHz frequency offset for the three carrier frequencies. In a $\Delta\Sigma$ fractional-N PLL, the out-of-band phase noise of the PLL is dominated either by VCO phase noise or $\Delta\Sigma$ modulator quantization noise [34]. Therefore, although the QN from $\Delta\Sigma$ modulation is suppressed by 6 dB, the out-of-band phase noise suppression of the PLL may not be as much as 6 dB, especially at high output frequency where VCO phase noise is dominant. The measured performance of the $\Delta\Sigma$ fractional-N PLL with the proposed glitch-free PS-MMFD is summarized in Table II and the performance comparison with two prior-art QN suppression frequency dividers [10], [11] is summarized in Table III.

IV. CONCLUSION

In this paper, a novel multi-modulus frequency divider architecture utilizing glitch-free phase switching is proposed to achieve half-stepped division ratios and thus QN suppression in fractional-N PLLs. Theoretical analysis and circuit implementations with practical timing issues discussions for the proposed PS-MMFD are presented in details. The proposed PS-MMFD is unconditionally glitch-free and achieves 6-dB QN suppression thanks to its half-step division. The proposed PS-MMFD is able to operate at higher input frequency and consume less current, compared with other state-of-the-art frequency dividers (usually based on double-edge-triggering technique) used for QN suppression. An experimental fractional-N PLL utilizing the proposed glitch-free PS-MMFD is designed and implemented in a 0.18-µm CMOS process. The measurement results demonstrate the expected out-of-band phase noise suppression provided by the proposed PS-MMFD. The chip area for the proposed PS-MMFD is 0.38 mm × 0.25 mm and the power consumption is 5 mA from a 1.8-V power supply when operating at an input frequency of 2 GHz.

REFERENCES