Fault Detection and Mitigation in Multilevel Cascaded Converter STATCOM's

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Abstract -- This paper introduces an approach to detect the existence of the faulted switch, identify which switch is faulty, and reconfigure the STATCOM. This approach is illustrated on an eleven-level STATCOM and the effect on the dynamic performance and the total harmonic distortion (THD) is analyzed Many static synchronous compensators (STATCOMs) utilize multilevel converters due to the following reasons lower harmonic injection into the power system; decreased stress on the electronic components due to decreased voltages; and lower switching losses. One main disadvantage, however, is the increased like- lihood of a switch failure due to the increased number of switches in a multilevel converter. single switch failure, however does not necessarily force an (2n+1) level STATCOM.Even with a reduced number of switches, a STATCOM can still Provide a significant range of control by removing the module of the faulted switch and continuing with (2n-1) levels.

Keywords-- Fault detection, multilevel converters, Static Synchronous Compensator (STATCOM).

I. INTRODUCTION

The Static synchronous compensator (STATCOM) plays a vital role in power systems. This is one of the Fact controllers which are used for controlling voltage regulation and reactive power compensation.STATCOM is capable of generating and absorbing reactive power and in which the output can be varied to control the specific parameters of an electric powersystem.STATCOM works in capacitive mode if it injects reactive power to the power system. It works in the inductive mode if it absorbs reactive power from the system.

If no reactive power exchanges between a STATCOM and a system, the STATCOM works in standby mode. There are several compelling reasons to consider a multilevel converter topology for the STATCOM.The well known reasons are

1)lower harmonic injection into the power system;

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2)decreased stress on the electronic components due to decreased voltages; and

3)lower switching losses.

4)The dynamic voltage control in transmission and distribution systems.

Generally STATCOM is composed of one inverter with energy storing capacitors on its dc side, inductances and a coupling transformer on its ac side, and a control system, is connected in parallel with the power grid as shown in fig 1.The STATCOM controls the reactive power flow in the electric line injecting or absorbing it. An eleven level cascaded multilevel STATCOM is shown in fig 2.This converter uses several full bridges on series to synthesize staircase waveforms. Because every full bridge can have three output voltages with different switching combinations, the number of output voltage levels is 2n+1 where n is the number of full bridges in every phase. The converter cells are identical.

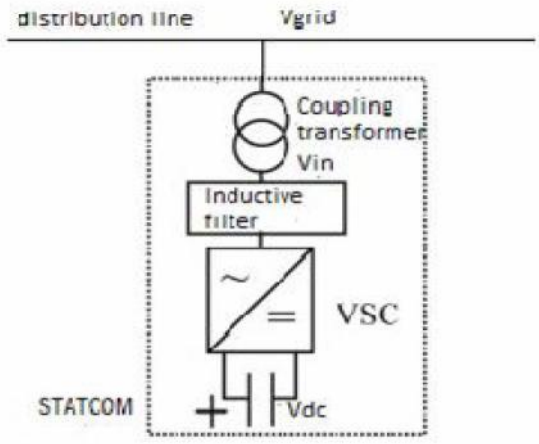


Fig 1. Single phase STATCOM

Higher level converters are used for high output rating applications .A large number of power switching devices will be used. All the multilevel converter topologies ,namely ,neutral point clamped converter, cascaded multicell, and flying capacitor type converter require a large number of components in order to distribute the voltage (and hence the

Fig 2. Eleven level cascaded multilevel STATCOM

power)among them. An associated issue related to a high number of components is an increase in the probability of internal fault. Therefore it is important to design a sophisticated control to produce a fault tolerant STATCOM.

A faulty power cell in a cascaded H-bridge STATCOM can cause fault conditions leads to the damage of the system .So, it is important to identify the existence and location of the fault for it to be removed. Converter malfunctioning may result in important fault conditions such as short circuit or an overvoltage applied to the supply and or to the load, explosion of switch modules, or system breakdown resulting in eventual time and economic loss. The study of causes, fault modes, and suitable protection strategies are necessary but are complex due to slow enough to be handled by the output inductor.

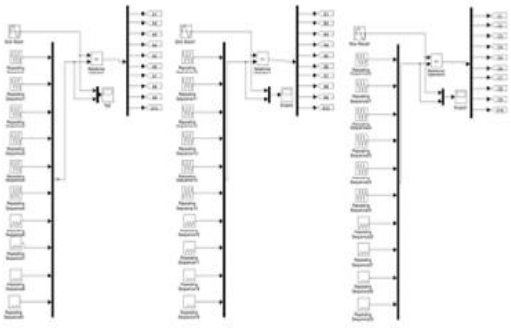


Fig 3. Phase Shift PWM Technique

The Primary drawback with the Proposed last few years approach is the fault detection time depends on the time constant of the load .Therefore for loads with a larger RL time constant the faulty Power cell can go undetected for the numerous cycles, potentially leading to circuit damage This paper mainly focus on the fault detecting and the module in which fault occurred is then isolated and removed from the service in the cascaded eleven level multilevel STATCOM.

This approach is consistent with the modular approach of cascaded converters in which cells are designed to be interchangeable and rapidly removed and replaced. This approach offers the following advantages:

- Not necessary to use additional sensing devices.
- Is inconsistent with the modular approach of cascaded multilevel converters and
- The dynamic performance and THD of the STATCOM is not significantly impact.

II.MULTILEVEL STATCOM

Multilevel Converters have been widely used in high voltage, high power applications in recent years. This is due to several advantages that they offer compare to the standard two level converter topology. In addition to these there use in low power applications. There are several topologies of multilevel converters. The most important are the Diode clamped converter, Flying capacitor and the cascaded connection of H bridges. This paper offers the cascaded multilevel STATCOM.

It consists of several H bridges in series to synthesize staircase waveforms. The inverter legs are identical and are therefore modular. In the eleven levels STATCOM, each leg has Five H Bridges. Since each full bridge generates three different level voltages (v,0,-v) under different switching states, the number of output voltage levels will be eleven, A multilevel configuration offers the several advantages over other converter types

1) Lower harmonic distortion of the output voltages and currents, the limitation of voltage transients, and the high efficiency across the power operation range.

2) It generates a multistep staircase waveform approaching a more sinusoidal output voltage by increasing the number of levels.

3) Multistage Cascaded Topologies using H-bridges are relatively few power devices and each of the bridges working at low switching frequency which gives the possibility to work at high power levels with low speed semiconductors and to generate low switching frequency losses its own dc source.

To achieve a high quality output voltage waveform, the voltage across all the dc capacitors should maintain a constant value. Variations in load cause the capacitors to charge and discharge unevenly leading to different voltages in each leg of each phase. However because of the redundancy in switching states Therefore there exists a best state among all the possible states that possible switching states that can be used to synthesize a given voltage level, the particular Switching topology is chosen such that the capacitors with the lowest voltages are charged and conversely, the capacitors with the highest voltages are discharged. This redundant state selection approach is used to maintain total dc link voltage to a near constant value and each individual cell capacitor within a tight bound. Different pulse width modulation (PWM) techniques have been used to obtain the multilevel converter output voltages. For cascaded converters phase shifted PWM is the most common strategy. This paper focuses on the PSPWM because of extensive use, ease of implementation.

This strategy leads to cancellation of all carrier and associated sideband harmonics up to the (n-1) th carrier group for a n level converter. Fig 2.illustrates the carrier and reference (level converter. Each carrier signal is phase shifted by $\Delta\emptyset=2\Pi/n$ frequency for PWM is in the range of 1- 10khz.Where n is the number of cells in each phase. The modulation of each cell is generated by comparison between a voltage reference and a triangular carrier which has a frequency fcr. To obtain the output voltage for vax+,the carrier is compared with unipolar voltage reference v, and if unipolar modulation is used, the ,the output voltage for vaxaxis obtained by comparing carrier with the negative voltage reference –v shown in figure 4

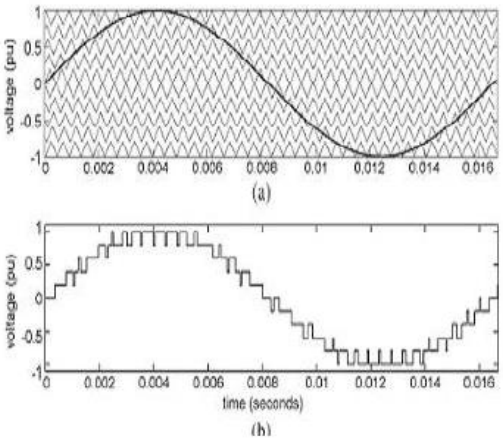


Fig 4. Carrier and reference waveform of PSPWM

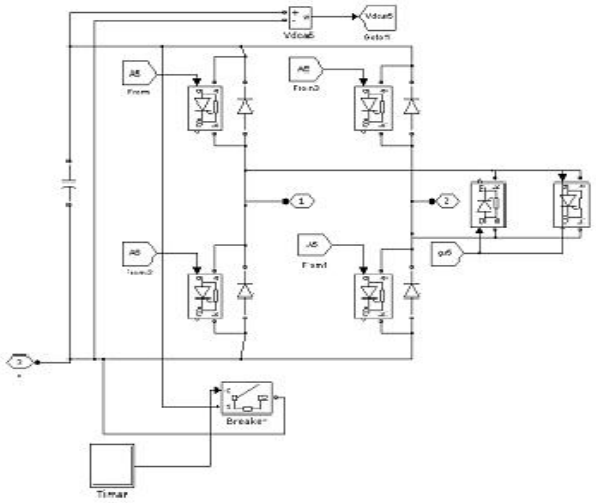


Fig 5. Cell with fault switch

III.FAULT ANALYSIS FOR THE MULTILEVEL STATCOM

A Converter cell block is shown in fig 5.can experience several types of faults. Each switch in a cell can fail either in open state or in closed state. Closed fault is most severe fault if compared with open fault since it may lead short circuit. An open circuit can be avoided by using a proper gate circuit to control the gate current of the switch during the failure occurs. It is obvious that when a power switch short circuit failure occurs, the source or capacitors will discharge through a conducting switch pair, if no switch action is taken. Hence the counterpart of the failed switch must be turned off quickly and properly to avoid system collapse due to a sharp current surge, On the other hand a power switch open circuit failure will cause a hazard by attempting to interrupt the load current, if no protective action is taken. The nomenclature of the proposed method is shown below.

Consider the simplified eleven-level converter is shown in fig 6.The process for identifying and removing the faulted cell block is shown in fig5.The input to the detection algorithm is Eout for each phase, where Eout is the STATCOM filtered RMS output voltage. If the STATCOM RMS output voltage drops below a preset threshold value(E1),then a fault is known to be occurred shown in fig 7. E1is the STATCOM threshold voltage (constant) Possible STATCOM output voltage xi Difference between possible and actual STATCOM output(V) Eout STATCOM output voltage E1 STATCOM threshold voltage (constant)(v) Sj1,Sj2 Switching signal of the j-th cell (0,1) bypass signal for j-th cell(0,1).

Eout is the Filtered STATCOM output voltage
f1=vdc0(s21-s22+s31-s32+ s41-s42+s51 -s52) (cell 1 faulted)
f2=vdc0(s11-s12+s31-s32+s41-s42+s51-s52) (cell 2 faulted)
f5= vdc0(s11-s12+s21-s22+s31-s32+s41-s42)

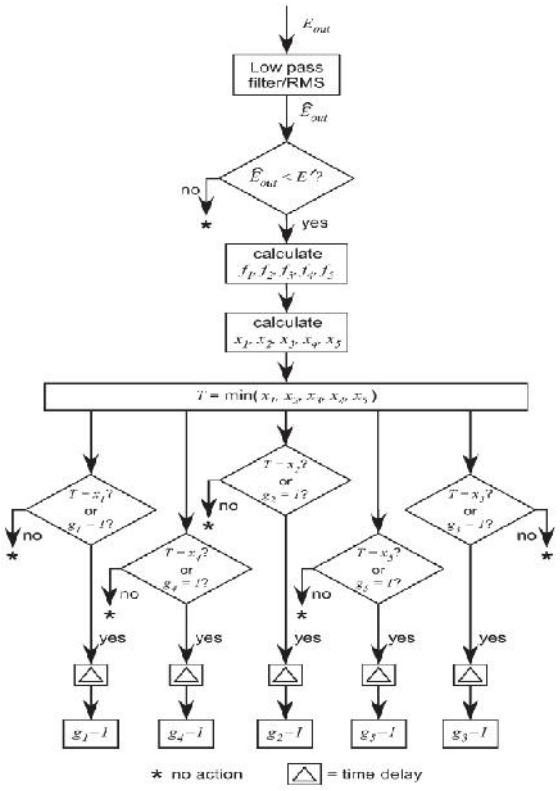


Fig 6: Flow Chart of an eleven level Converter

Where Vdc0 is the ideal voltage across a single cell block. If there is a fault cell only one will be near the actual STATCOM output phase voltage Eout. All of the others will be too high. Therefore to determine the location of the fault cell, each is compared against Eout to yield Xi=|Eout-fi|, i=1.2……..n.

The smallest xi indicates the location of the faulted block because this indicates the fi which most closely predicts the actual .The choice of threshold voltageE1depends on the number of cells in the converter The ideal output voltage is Fig 7: Flowchart for eleven level converters Eout,0=nVdc0/√2 During fault ,Eout will decrease by Vdc0 yielding,

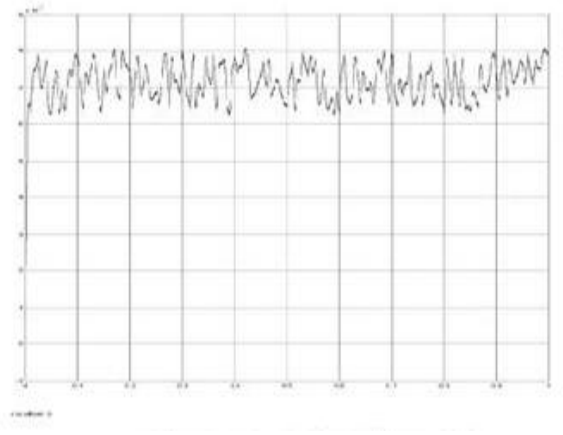
$$E = n - 1\ Vdc0\ \sqrt{2}$$

Therefore, the threshold voltage E1 should be chosen such that (n-1/n) Eout,0<E1<Eout,0.In an eleven level converter=5 and the faulted RMS voltage will decrease by roughly 20%.Therefore a good choice for E1 is 85% of the rated output STATCOM voltage.

The last step is to actuate the module bypass switch shown in fig.5.A slight time delay is added to the logic to neglect for momentary spikes that may occur. It is desirable to neglect momentary sags in voltage, but respond to sags of increased duration that indicate a faulted module.

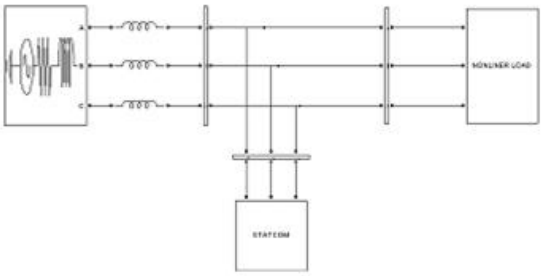
IV.EXAMPLE AND RESULTS

The line diagram of electrical arc furnace load is shown in fig.8.Because the harmonics generated by a DC arc furnace are mostly determined by its AC/DC converter and the characteristic is More predictable. Electric arc furnaces are commonly encountered in steel plants .Due to the uncontrolled nature of the steel melting process, current harmonics generated by the arc furnaces are unpredictable and random. Fig depicts the typical arc furnace system supplied by an arc source. The source impedance Xsc is small. The substation transformer HV/MV connects the high voltage bus to the medium voltage bus .The furnace transformer MV/LV connects the medium voltage bus to the arc furnace electrodes. There may be other loads connected to the two buses. The arc furnace load impedance includes the series of Xel and Rel. Due to the current chopping and igniting in each half cycle of the supply voltage; arc furnaces generate a wide range of harmonic frequencies. Fig shows the arc current and voltage when sinusoidal source supplies the furnace. the line active power drawn by the arc furnace load is shown in fig 7.



V.DYNAMIC PERFORMANCE

To test the To test the Proposed fault detection and mitigation approach ,a approach a faulty power cell was initiated at 2.5s.with in 300ms,the fault has been detected ,the module removed and necessary; the fault was intentionally left on to better illustrate its effect on the effect system and removal. The STATCOM bus voltage and line ac and line active power are shown before the fault, during and after the faulty module is removed. Shown in fig 8 and 9 .Note that both the bus voltage and line active power are adversely affected during the fault. In both cases, the high frequency oscillations are increased. Once the faulty cell is removed, the system returns to its Perrault behavior. There is a small induced low-frequency oscillation that can be observed in the line active power, but this is rapidly damped by the STATCOM's control.



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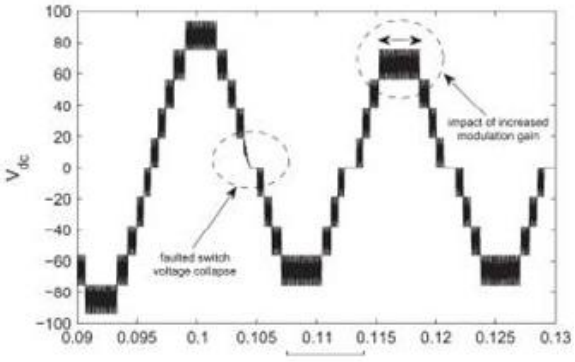

There are several important aspects of this output waveform that have been highlighted. Note that the voltage collapse of the first level due to the faulted cell. This collapse in voltage will occur at the level that corresponds to the faulty cell. It is not possible to directly correlate the level number with the cell number because of the redundant state selection scheme that is used to balance the capacitor voltage.

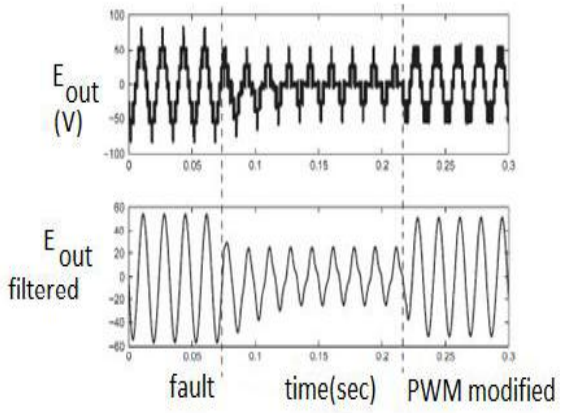

Fig 10.Experimental STATCOM dynamics change in PWM

A further aspect of note is the increase in length of the top level duration .This is due to the increase in the modulation gain k due to the decrease in dc link voltage. Since the STATCOM output voltage is directly proportional to Vstat=kVdccos α Where k is the modulation gain and α is the phase angle.

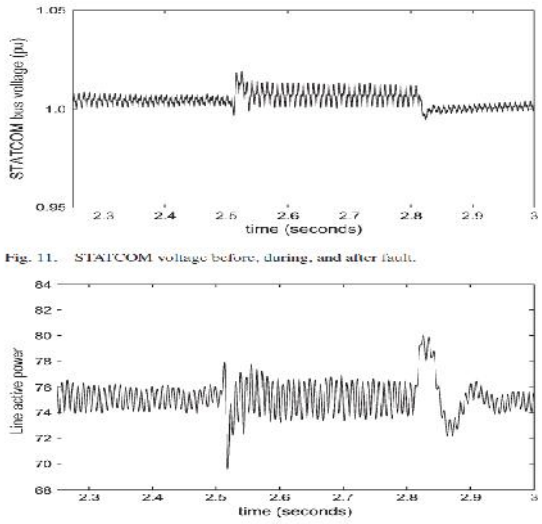

Fig. 11. STATCOM voltage before, during, and after fault.

VI.THD PERFORMANCE

Harmonic analysis has been performed on the output voltage at the point of common coupling. One of the primary reasons for using a multilevel converter is the reduction in harmonic content in the output waveform. Before the fault, the THD level is less than 1%, which is quite good. During the fault THD increases over 5%.When the fault is removed

THD decreases and settles at approximately 2.5%,which is inacceptable range for a 115-KV.

VII.EXPERIMENTAL RESULTS

For this prototype, Three H Bridge cells are cascaded to make a seven level inverter for each phase of the STATCOM. During normal operation the capacitor voltage for each cell is 30V.The output voltage of the converter during the normal operation, during the fault, and after removing the faulty cell is depicted in fig.13sfault is applied to the second cell at point "F" as shown in fig with dashed line. Immediately after the fault is applied, the block capacitor begins to discharge. The capacitor voltage is shown in .Fig (c) shows the output of the fault detection algorithm. When a fault is detected , g2(gate signal of the bypass circuit)becomes activated and triggers the bypass of the second cell and deactivates the PWM commands to the faulty H bridge. Fig (d) shows the filtered output of the STATCOM.

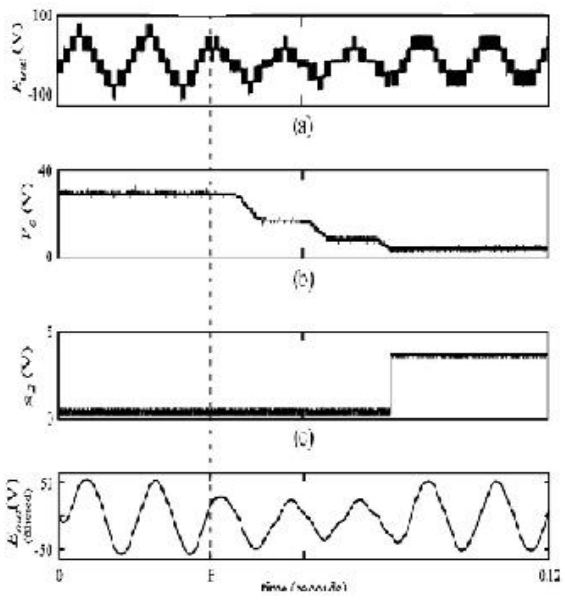

Fig 13:Experimental STATCOM dynamics before, during, and after a fault is applied; (a) *E*out, (b) capacitor voltage at faulted cell, (c) gating signal of cell 2 by-pass switch, and (d) *E*out (filtered).

CONCLUSION

In this paper, a fault detection and Mitigation strategy for a multilevel cascaded converter has been proposed. This approach requires no extra sensors and only one additional bypass switch per module per phase. So this is considered as the one of the main advantage as compared with conventional systems. The approach has been validated on a 115-kV system with a STATCOM compensating an electric Non linear load. This application was chosen since the arc furnace provides a severe application with its non sinusoidal, unbalanced, and randomly fluctuating load. The proposed approach was able to accurately identify and remove the faulted module. In addition, the STATCOM was able to remain in service and continue to provide compensation without exceeding the total harmonic distortion allowances.

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