Simulation Based Analysis of Seven Level Cascaded Multilevel Inverter

V. S. Bharath and M. Gopinath

Abstract: In this paper, the topology of multilevel inverter has been developed in order to achieve the balance control method application. Multilevel Inverters are very popular and have many applications in electric utility and for industrial drives. In this paper, the THD contents of seven level cascade multilevel inverters have been analysed. When this Multilevel inverter are used for industrial drive directly, the THD contents in output voltage of inverter is very significant index as the performance of drive depends very much on the quality of voltage applied to drive. A MATLAB/Simulink model of an inverter was used for the Simulation analysis.

Keywords — Cascade multilevel inverter, harmonic elimination, modulation index, switching angles, total harmonic distortion.

I INTRODUCTION:

In the recent years especially in the distributed energy resources area, multilevel inverters have been drawing growing attention due to the fact that several batteries, fuel cells, solar cell, wind, and micro turbines can be connected through a multilevel inverter to feed a load or the ac grid without voltage balancing problems. The ac output voltage obtained from the inverters can be fed to a load directly without voltage balancing problems. To reduce the harmonics further, different multilevel sinusoidal PWM and space-vector PWM schemes are suggested in the literature [1]. The multilevel inverters offer many advantages as compared to two-level pulse width modulation inverters, such as their capabilities to operate at high voltage with lower dv/dt per switching, high efficiency, low electromagnetic interference etc [2]-[4]. As a result it is possible to apply symmetric charging methods in symmetric cascaded multilevel inverters [5]–[7]. Previous work [8]-[10] has suggested that multiple inverter islands may behave differently depending on the system configuration. In the present work, seven level CMLIs are employed to generate ac output voltage producing different magnitudes of THD at different values of modulation indices for comparison purpose. The switching angles have been computed by the implementation of Newton Raphson (N-R) numerical technique in a particular way producing complete solutions for working range of modulation index without much computational complexity.

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II SEVEN LEVEL CASCADED MULTILEVEL INVERTER.

The cascade multilevel inverter consists of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series. Each H-bridge can produce three different voltage levels: +Vdc, 0 and –Vdc by connecting the dc source to ac output side by different combinations of the four switches S1, S2, S3, and S4. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs. By connecting sufficient number of H-bridges in cascade and using proper modulation scheme, a nearly sinusoidal output voltage waveform can be synthesized. The number of levels in the output phase voltage and line voltage are 2s+1 and 4s+1 respectively, where s is the number of H-bridges used per phase. For example, three H-bridges per phase are required for 7-level multilevel inverter respectively. Fig.01 shows 7-level multilevel inverter and Fig.02 shows a typical waveform produced by 7-level CMLI.

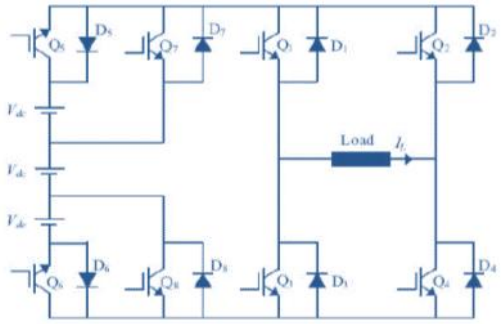

Fig.01: Seven Level Multilevel Inverter

In the Fig.02, α1, α2 and α3 are the switching angles for three H-bridges in each phase, and β1, β2 and β3 are corresponding supplementary angles for α1, α2 and α3. The magnitude and THD content of output voltage depends very much on these switching angles, therefore, these angles need to be selected properly.

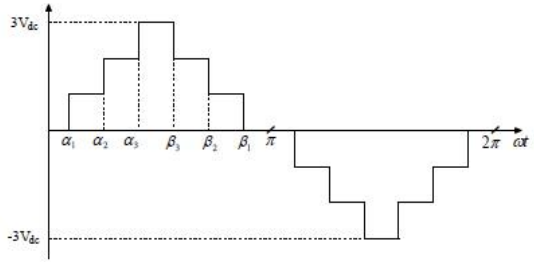

Fig.02: Output phase voltage waveform for 7-level CMLI

III SWITCHING MODEL.

In order to verify the ability of the proposed multilevel inverter topology to synthesize an output voltage with a desired amplitude and better harmonic spectrum, programmed PWM technique is applied to determine the required switching angles. It has been proved that in order to control the fundamental output voltage and eliminate n harmonics, therefore n+1 equation is needed. Therefore, 7-level inverter, for example, can provide the control of the fundamental component beside the ability to eliminate or control the amplitudes of two harmonics, not necessarily to be consecutive. The method of elimination will be presented for 7-level inverter such that the solution for three angles is achieved. The Fourier series expansion of the output voltage waveform using fundamental frequency switching scheme is as follows:

$$V(\omega t) = (4vDC/\pi)\,\Sigma\,[\cos(n\theta 1) + \cos(n\theta 2) + \ldots\ldots\ldots + \cos(n\theta s)]\sin(n\omega t) \text{ ---------- (1)}$$

where n = 1, 3, 5, 7,...

Where s is the number of dc sources in the multilevel inverter. Ideally, given a desired fundamental voltage V1, one wants to determine the switching angles θ1, θ2, θ3…

IV SIMULATION RESULTS.

The feasibility of the proposed approach is verified using computer simulations. A model of the seven-level inverter is constructed in MATLAB-Simulink software. A new strategy with reduced number of switches is employed. For cascaded H bridge 7 level inverter requires 12 switches to get seven level output voltage and with the proposed topology requires 8 switches. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels The schematic of the cascaded H bridge seven level inverter built in MATLAB-Simulink is illustrated in Fig.03. The switching patterns adopted are applied for the proposed topology and switches to generate seven output voltage levels at 0.9 modulation index and the switching pattern are shown in the Fig.04. Simulation results for 7-level inverter at Vdc=50Vs, ma=0.9 where s=3 and corresponding output voltages for proposed seven level inverter are shown in Figs.05.

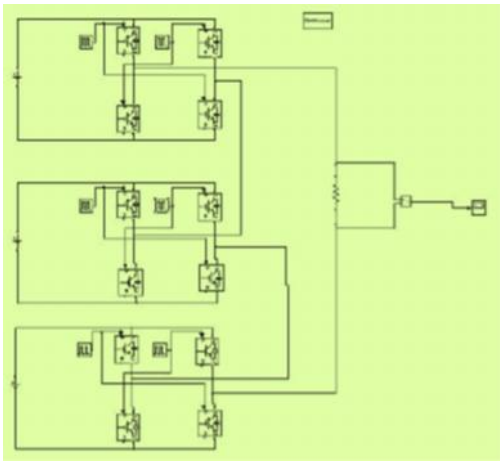

Fig.03. Simulation Circuit of 7-level CMLI

Fig.04. Switching pattern of seven level inverter

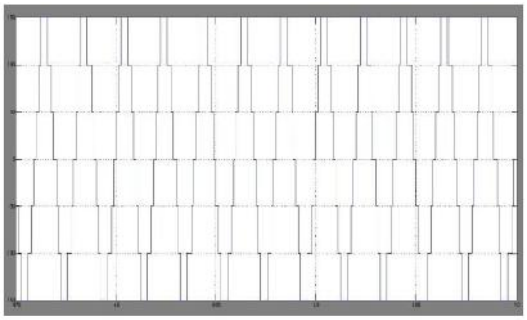

Fig.05. Output Voltage of Inverter

By using N-R method, all possible solution sets for a 7-level CMLIs are computed and a complete analysis is presented. For 7-level CMLI, two switching angles have been calculated as shown in Fig.06. It can be seen that for some values of *m* solutions do not exist, for some other values of *m*, multiple solutions exist and simple solution exists for most of the values of *m*. Some typical values of switching angles (in radians) are given in Table I.

m	α_1	α_2	α_3
0.2710	0.8120	1.4755	1.5410
0.5000	0.6881	0.9818	1.3980
0.6000	0.2064	0.7280	1.4960
0.8400	0.2729	0.3273	0.9146
0.9200	0.1394	0.2672	0.6348

Table: 01 Values of switching angles.

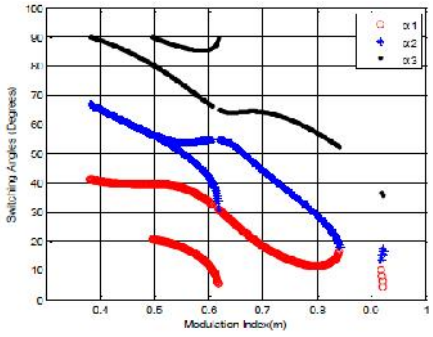

Fig.06.Switching angle vs. modulation index

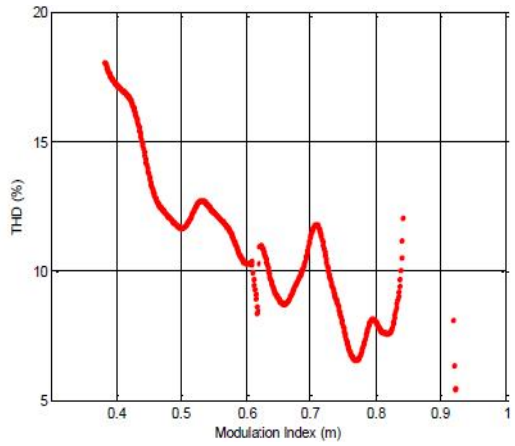

Fig.07.THD vs. modulation index

For each of the multiple solution sets as computed above, total harmonic distortion (THD) in percentage is computed according to equation (2), for 7-level CMLI x=11. The set of switching angles among multiple solutions which produce least THD is selected for switching of semiconductor devices, and these are termed as combined solutions. The THD plots for solution are plotted as a function of *m* in Fig.07. It can be seen from the Fig.07, that THD is more than 5% for all values of modulation indices, hence not satisfying IEEE-519 standard. This type of output voltage cannot be used directly for power system and industrial drive applications due to high THD.

$$THD = \frac{\sqrt{\sum_{n=x}^{n=49} V_n^2}}{V_1} \times 100 \quad \text{-----(2)}$$

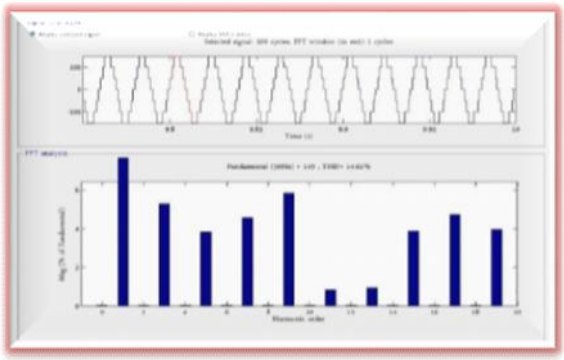

Fig.08. FFT Analysis

The proposed topology has the advantage of its reduced number switches and harmonics are reduced with THD value of 14.62 at 149V is achieved. For proposed harmonic spectrum of the simulation system is as shown in the Fig.08, which shows the results are well within the specified limits of IEEE standards. The results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB.

V CONCLUSION.

A new family of multilevel inverters has been presented and built in MATLAB-Simulink. It has the advantage of its reduced number of switching switches. The switching angles for cascade multilevel inverters of 7-level have been computed for analysis of total harmonic distortions produced in output voltage and complexity in computation of these angles. It has been found that the THD in output voltage decrease and output voltage increase with increase in number of levels. The simulation results show how effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the output voltage THD.

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