Three Level Neutral Point Clamped Back to Back Converter

L. Sai Suman Rao and S. Nagaraja Rao

Abstract--- Generally voltage source multilevel power converter structures are being consider for high power high voltage application where they have well known advantages. Recently back to back multilevel neutral point clamped converters have been used in high voltage direct current transmission systems. Bipolar back to back connections of neutral point clamped converter have advantages in long distance HVDC transmission systems, but it is difficult to balance the DC capacitor voltage dividers. The project proposes voltage balance control of three level converter with sinusoidal pulse width modulation for back to back AC to DC to AC converter. It consists of a forced commutated rectifier at one end and a force commutated inverter at other end with a common DC-link. In the proposed back to back converter each converter is controlled independently. The input is directly given to the multilevel rectifier section. The need for the multilevel in the input side is to reduce the current input in the supply. The back to back topology requires doubling the number of switching devices. It has advantages of (I) Lower input current harmonics (II) Ability to control the voltage of the DC-bus and (III) Bidirectional Power flow control. The multilevel converter section used here is three levels. The proposed system is to be simulated by using MATLAB simulink.

Index Terms-- Multilevel concept, Neutral Point Clamped Converter, Total harmonic distortion, Voltage Balancing.

I. INTRODUCTION:

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.

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Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies.

Input current: Multilevel converters can draw input current with low distortion.

Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

The selection of the best multilevel topology for each application is often not clear and is subject to various engineering tradeoffs. By narrowing this study to the DC/AC multilevel power conversion technologies that do not require power generation.

II. SYSTEM CONFIGURATION:

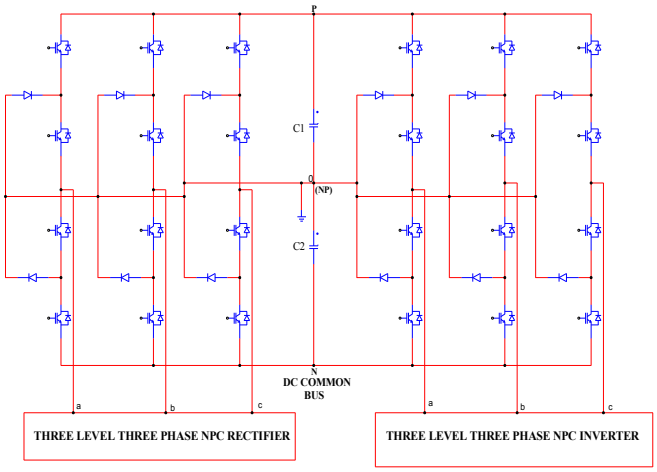


Fig1. Three-level three-phase back-to-back converter.

When interconnecting two diode-clamp multilevel converters together with a %c capacitor link," the left-hand side converter serves as the rectifier for utility interface, and the right-hand side converter serves as the inverter to supply the ac load. Each switch remains switching once per fundamental cycle. The result is a well balanced voltage across each capacitor while maintaining the staircase voltage wave, because the unbalance capacitor voltages on both sides tend to compensate each other. Such a dc capacitor link is categorized as the "back-to-back intertie."

The purpose of the back-to-back intertie is to connect two asynchronous systems. It can be treated as
(1) Lower input current harmonics,
(2) Ability to control the voltage of the DC-bus and
(3) Bidirectional Power flow control. The power flow between
two systems can be controlled bidirectionally.

III. THREE LEVEL DIODE CLAMPED INVERTER:

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m level diode-clamp inverter needs (m-1) capacitors on the DC bus. A three-phase three-level diode-clamped inverter is shown in Fig. 2 In this circuit, the DC bus voltage is split in to three levels by two series connected bulk capacitors C1 and C2. The middle point of the two capacitors 'n' can be defined as the neutral point. The diodes Da1 and Da2 clamp the switch voltage to half the level of the DC bus voltage.

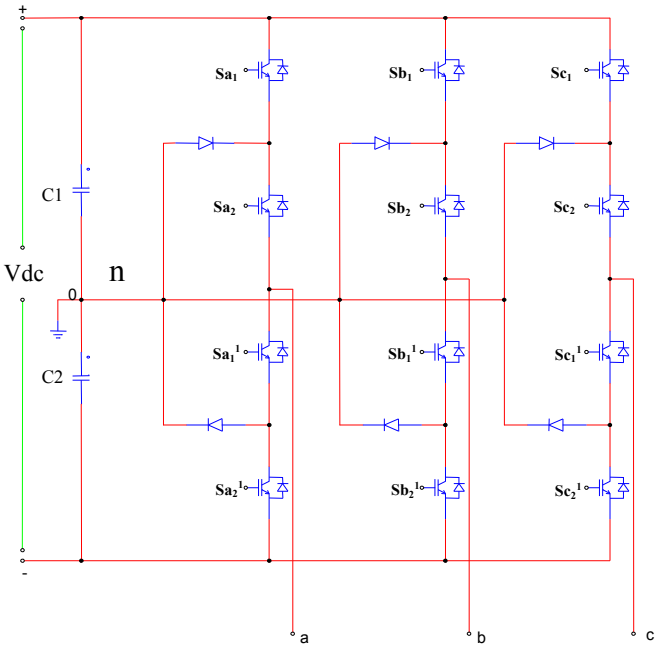
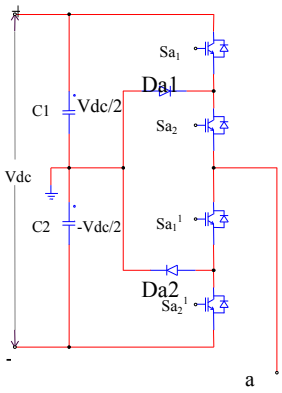


Fig 2. Three-phase three level diode clamped inverter

one phase of three level diode clamped inverter to produce a stair case output voltage, let us consider only one phase of the three level inverter as shown in the Fig 3(a). Fig 3(b) provides a three level output across 'a' and 'o' i.e., Vao=0, Vdc/2, -Vdc/2.



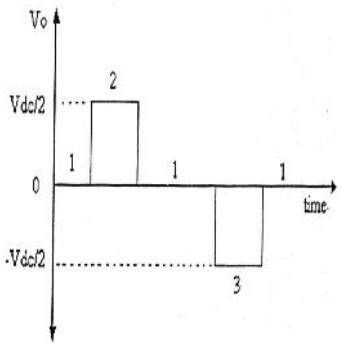


Fig 3(a). One phase of three level diode clamped inverter
Fig 3(b). Output waveform of one phase DC3LI

Table of Switching state for DC3LI

OUTPUT VOLTAGE V_{ao}	SWITCHING SEQUENCE			
	S_{a1}	S_{a2}	S_{a1}^1	S_{a2}^1
0	0	0	0	0
$V_{dc}/2$	1	1	0	0
$-V_{dc}/2$	0	0	1	1

IV. THREE LEVEL DIODE CLAMPED RECTIFIER:

The proposed circuit configuration is based on the three-phase, three-leg neutral point clamped converter shown in Figure 4. The converter consists of a boost inductor Ls on the ac side, to filter the input harmonic current and achieve sinusoidal current waveforms. Rs is the series equivalent resistor. Twelve switching devices with rating Vdc / 2 and six clamping diodes with the rating of Vdc / 2 are used. The diodes are used to clamp the dc-voltage. The converter also consists of two capacitors on the dc terminal. va, vb, vc represents the phase voltages of the three-phase AC system.

In Figure 4. Sa^1,Sa^2,Sa_1^1,Sa_2^1 are the four switching devices for phase A and similarly phase B and C have four switching devices. D_{1a},D_{2a},D_{1b},D_{2b},D_{1c},D_{2c} are the six clamping diodes. Rs,Ls are the input side resistance and the boost inductors, R_L is the load resistance connected across the two capacitors. C_1,C_2 are the output side DC capacitors to hold the dc output voltage. V_a,V_b,V_c are the three input supply voltages, i_a,i_b,i_c are the input phase currents, and I_3,I_2,I_1 are the three output node currents which charge the capacitor.

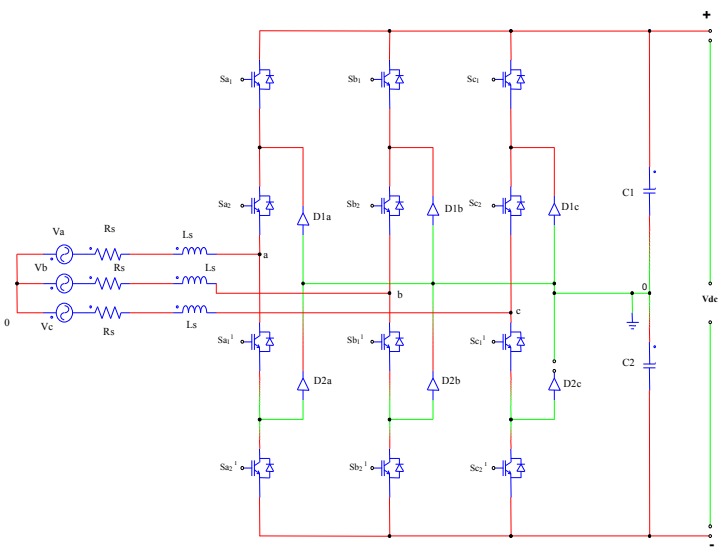


Fig 4. **Three-phase three level diode clamped Rectifier**

$$P^* = \frac{3}{2}\left(V_q^e I_q^e + V_d^e I_d^e\right)$$
$$Q^* = \frac{3}{2}\left(V_d^e I_q^e - V_q^e I_d^e\right)$$

By solving P^* and Q^* for I_q^e and I_d^e

$$I_q^e = \frac{3}{2\Delta}\left[P^* V_q^e + Q^* V_d^e\right]$$
$$I_d^e = \frac{3}{2\Delta}\left[P^* V_d^e - Q^* V_q^e\right]$$

Figure 5. shows the schematic of the control scheme. The voltage control is called the outer control loop and the current controllers are the inner control loop. Hence the time response of the current controllers has to be faster than that the voltage controller by at least 10 times. In the control scheme

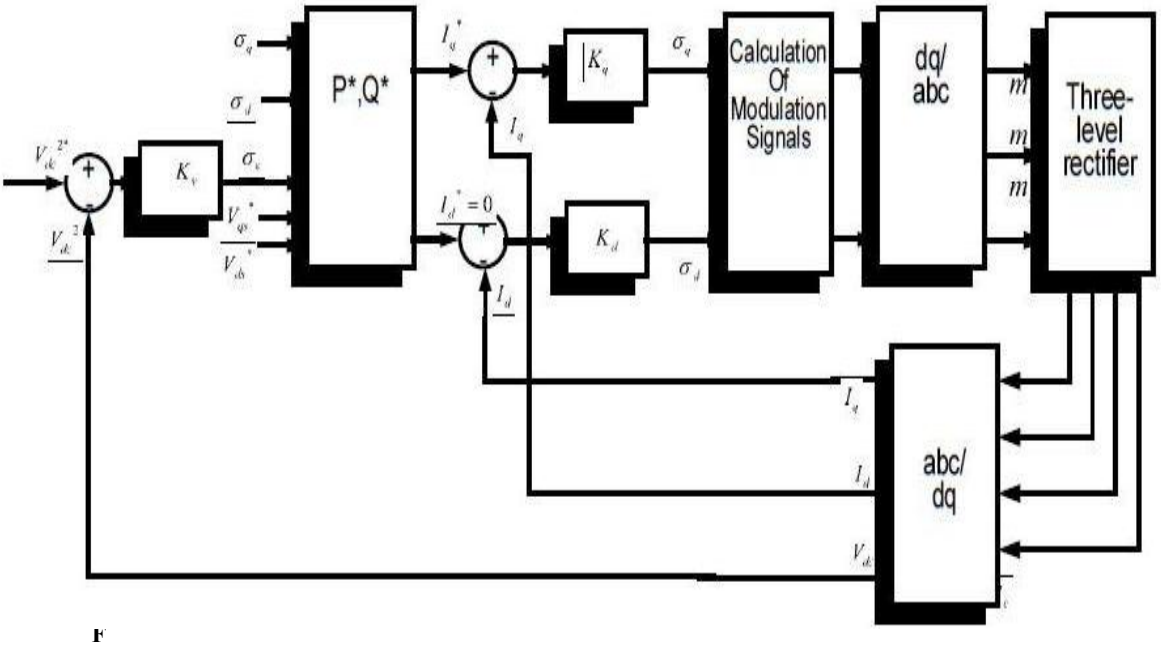


Fig 5. Block diagram of the control scheme

V. CONTROL OF THE CONVERTER:

The analysis and the control is done in a dq reference frame; i.e., all the quantities such as the voltages, currents, etc., are transformed to another reference frame so as to make the time varying quantities to be time invariant quantities. Controlling the time invariant quantities is simple and can be achieved using a PI, PD, or PID controller. In the following control scheme a cascaded control structure is being used, i.e., the output of one controller is used to calculate the reference of the other controller. Hence the time response of the controllers becomes a main criterion in designing the control parameters.

The active and reactive power for a three-phase balanced system is the square of the actual dc voltage V_{dc}^2 is compared with the reference dc voltage V_{dc}^{*2}. The error signal is passed through a PI controller K_v whose structure is explained in the next section. The output of this controller is assumed as σ_v. The reference q-d currents and can be calculated. These reference currents are compared with the actual q-d currents I_q^* and I_d^* can be calculated. These reference currents are compared with the actual q-d currents. The errors are passed through the two current controllers K_q and K_d. The outputs of these controllers are assumed as σ_q and σ_d. These q-d signals can be transformed back to the a-b-c reference frame to obtain the actual modulation signals. The carrier based PWM is used to obtain the gating signals for the devices. These modulation signals when compared with the two triangles, the switching functions for the devices can be obtained.

VI. BACK TO BACK CONNECTION FOR VOLTAGE CONTROL BALANCE:

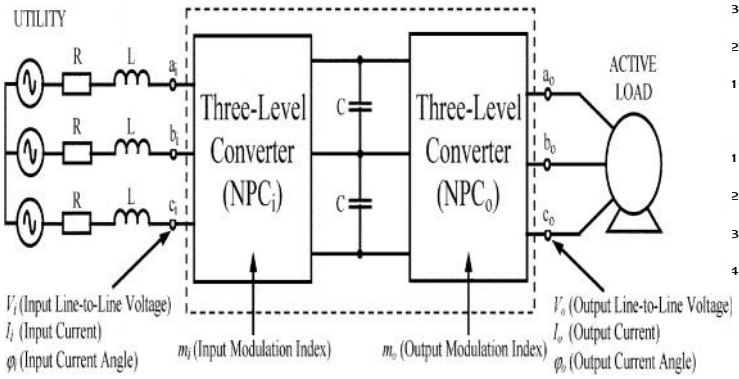


Fig 6. Back-to-back application of NPC converters.

The diode-clamped multilevel converter could not have balanced voltages for real power conversion without sacrificing output voltage performance. Thus, diode-clamped multilevel converters are suggested to be applied to reactive and harmonic compensation to avoid the voltage balancing problem.

The voltage unbalance problem could be solved by using a back-to-back rectifier/converter system and proper voltage balancing control.

VII. SIMULATION RESULTS:

Sinusoidal Pulse Width Modulation (SPWM):

In multilevel case, PWM techniques with three different disposed triangular carriers were proposed as follows:

- Alternate phase disposition (APOD) – every carrier waveform is in out of phase with its neighbor carrier by 1800.
- Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 1800 out of phase with those below zero.
- Phase disposition (PD)- All carrier waveforms are in phase.

In this project is focused only on all the carriers are in phase (Phase disposition)

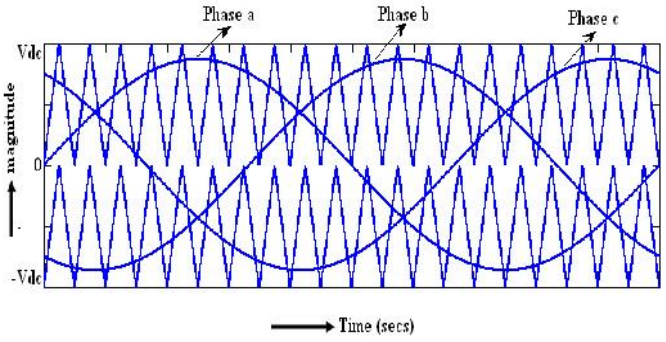
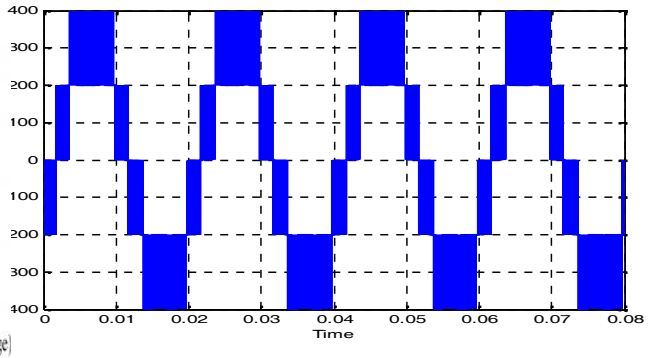
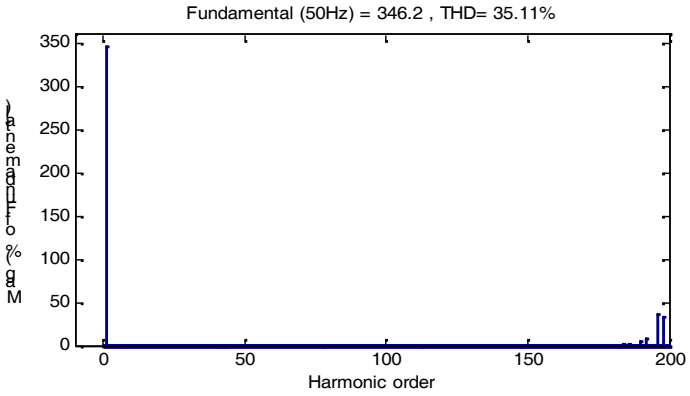


Fig 7. SPWM with triangular multilevel carriers

A. INVERTER SECTION



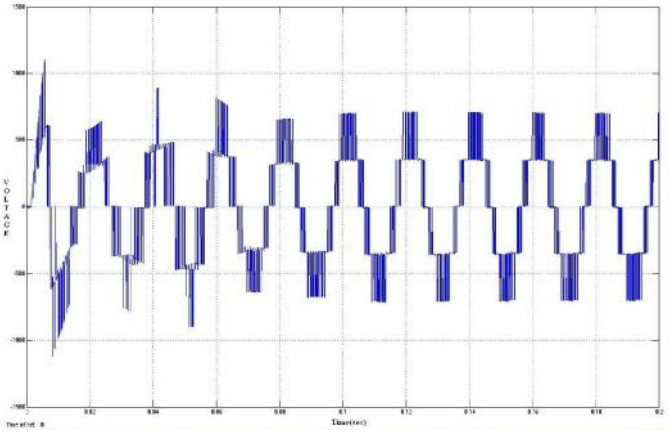
(a)



(b)

Fig 8. Three Level Diode Clamped MLI. (a) line voltage of Three level DC MLI. (b) THD of SPWM for Three level DC MLI

B. RECTIFIER SECTION



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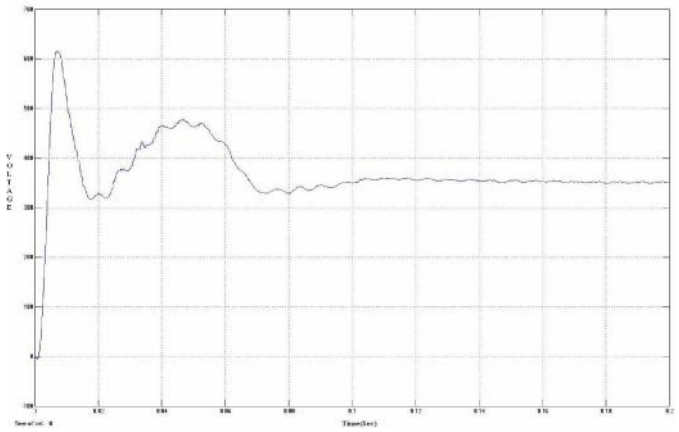

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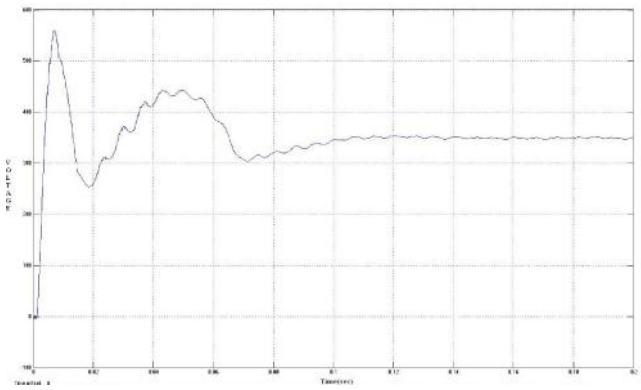
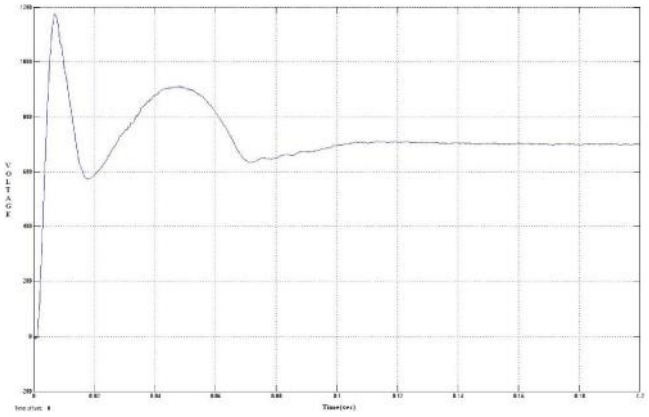
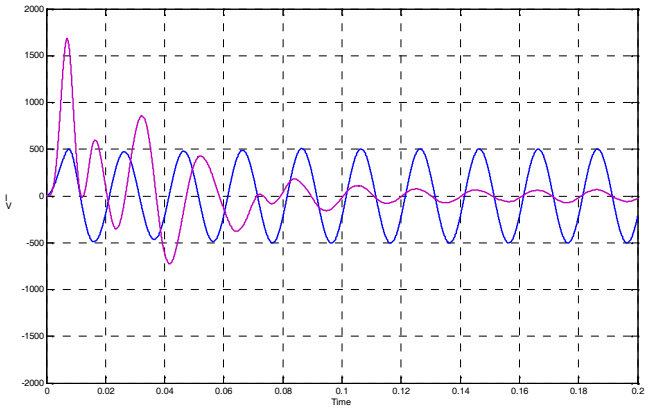


(c)

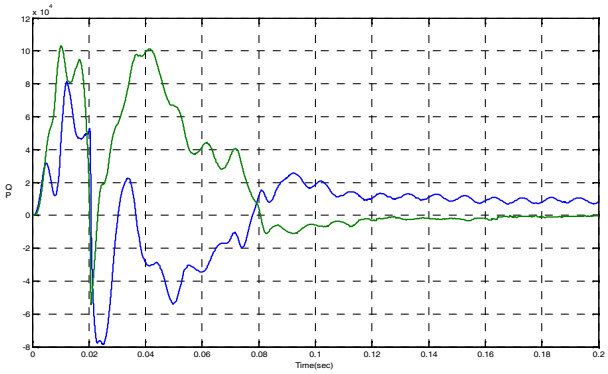


(d)

Fig 9. Three Level Diode Clamped MLR. (a) line voltage of Three level DC MLR. (b) Vc_1. (c) Vc_2. (d) DC Voltage Vdc.



(a)



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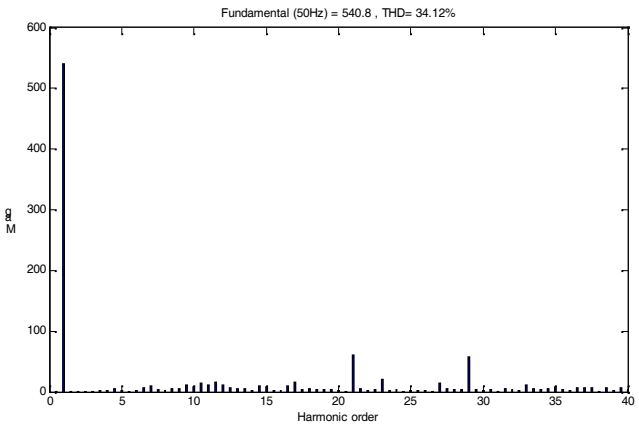

(c)

Fig 10. Three Level Diode Clamped MLR. (a) Vabc & Iabc. (b) Active and Reactive Power. (c) THD of SPWM for Three level DC MLR

CONCLUSION

In this paper, a control theory for the charge balancing of the Three-level NPC Converter system has been presented. Simulation and experimental results show that there is an equivalent performance between the two modulation strategies.

1) It can generate a three-level line-to-line staircase waveform, the Three-level converter generates sinusoidal

voltage and current waveforms even at fundamental switching frequency.

2) The voltages on the dc link capacitors are well balanced with very small ripple.

3) The system has low harmonics in the input current. The total harmonic distortion (THD) of input current was as low as 34.12% at full load with fundamental switching frequency using the pulse width modulation (PWM) control.

4) Each switch in the converter can switch only once per cycle when performing fundamental frequency switching; this results in high efficiency.

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