

Cascaded H-Bridge Multilevel Inverter Using Inverted Sine Wave PWM Technique

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Abstract: This paper proposes three phase Seven Level Cascaded H-Bridge Multilevel Inverter by using PD, POD, APOD, INVERTED SINEWAVE methods based on Sinusoidal PWM control techniques. There are 3 types of multilevel inverters named as diode clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter. Compared to diode clamped & flying capacitor type multilevel inverters cascaded H-bridge multilevel inverter requires least no of components to achieve same no of voltage levels and optimized circuit layout is possible because each level have same structure and there is no extra clamping diodes or capacitors. However as the number of voltage levels m grows the number of active switches increases according to $2 \times (m-1)$ for the cascaded H-bridge multilevel inverters. By comparing the three methods the performance parameters are calculated. Performance analysis is based on the results of simulation study conducted on the operation of the multilevel inverters using MATLAB/ SIMULINK. The performance parameters chosen the work included fundamental output voltage and total harmonic distortion.

Index Terms- Multilevel concept, Cascaded Multi level inverters, Total Harmonic Distortion.

I. INTRODUCTION

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive application of this technology is in the medium-to-high-voltage range, motor drives, power distribution, and power conditioning applications. In recent years, industry demands power in the megawatt level. Controlled ac drives in the megawatt range are usually connected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels.

In general multilevel inverter can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels. The main advantages of this approach are summarized as follows:

- They can generate output voltages with extremely low distortion and lower (dv/dt) .
- They draw input current with very low distortion.
- They can operate with a lower switching frequency.

- Their efficiency is high (>98%) because of the minimum switching frequency.
- They are suitable for medium to high power applications.

The selection of the best multilevel topology for each application is often not clear and is subject to various engineering tradeoffs. By narrowing this study to the DC/AC multilevel power conversion technologies that do not require power generation.

Multilevel inversion is a power conversion strategy in which the output voltage is obtained in steps thus bringing the output closer to a sine wave and reduces the total harmonic distortion (THD). Various circuit configurations namely diode clamped, flying capacitor and cascaded, etc., have been proposed [5].

II. SYSTEM CONFIGURATION

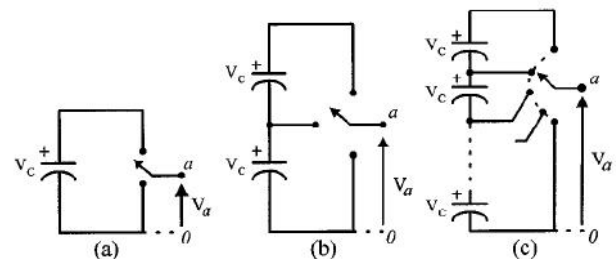


Fig .1. Multilevel concept for (a) two level (b) three level and (c) n- level

Multilevel inverter structures have been developed to overcome shortcomings in solid-state switching device ratings so they can be applied to higher voltage systems. The multilevel voltage source inverters [10] unique structure allows them to reach high voltages with low harmonics without the use of transformers. The general function of the multilevel inverter is to synthesize a desired ac voltage from several levels of dc voltages as shown in Fig.1.

Table.1. compares the power component requirement per phase leg among the two multilevel voltage source inverters mentioned above. The table shows that the number of main switches and main diodes needed by the inverters to achieve the same number of voltage levels is the same.

Multilevel Inverter Configurations	Cascaded Inverter(per phase)
Main switching Devices	2(m-1)
Main diodes	2(m-1)
Clamping diodes	0
Dc bus capacitors	(m-1)/2
Balancing Capacitors	0

Table.1

. Component requirements per leg of Cascaded Multilevel inverters

Conducting switches	Load voltage(Vab)
S1,S2	+Vdc
S3,S4	-Vdc
S1,S4 or S3,S2	0

Table.2. load voltage with corresponding conducting switches

II. CASCADED H-BRIDGE INVERTER

The cascade H-bridge inverter is a cascade of H-bridges, or H-bridges in a series configuration. A single H-bridge inverter is shown in fig (1) and three phase cascaded H-bridge inverter for seven-level inverter is shown in fig (2). Fig (1) and fig (2) shows the basic power circuit of single H-bridge inverter and the cascade of H-bridge inverter for seven-level inverter respectively. An N level Cascaded H bridge inverter consists of series connected (N-1)/2 number of cells in each phase. Each cell consists of single phase H bridge inverter with separate dc source. There are four active devices in each cell and can produce three levels 0, Vdc/2 and -Vdc/2. Higher voltage levels can be obtained by connecting these cell in cascade and the phase voltage van is the sum of voltages of individual cells, $v_{an} = v_1 + v_2 + v_3 + \dots + v_N$. For a three phase system, the output of these cascaded inverters can be connected either in Y or Δ configuration.

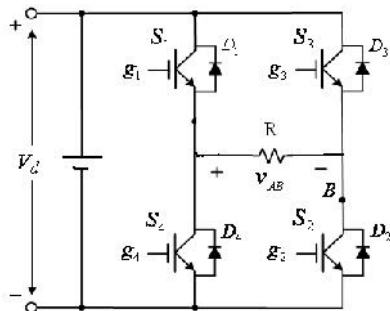


Fig (2) Configuration of single-phase H-bridge inverter

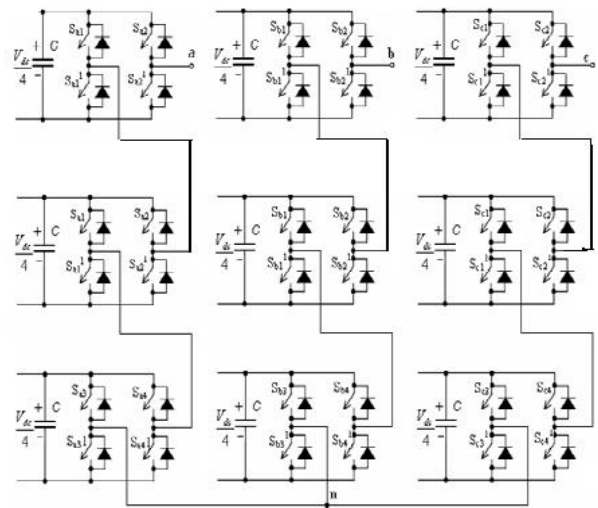


Fig 3 Configuration of three-phase Cascaded Seven Level H-Bridge Inverter (CH7LI)

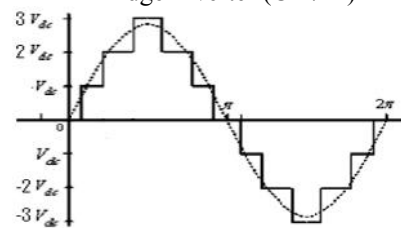


Fig. 4 Output wave form of single phase 7 level cascaded inverter

Output Voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
0vdc	1	0	1	0	1	0	1	0	1	0
Vdc	1	0	0	1	0	0	1	1	0	0
2vdc	1	0	0	1	0	0	1	1	1	0
3vdc	1	0	0	1	1	0	0	1	1	0
-vdc	0	1	1	0	1	1	0	0	1	1
-2vdc	0	1	1	0	0	1	1	0	1	1
-3vdc	0	1	1	0	0	1	1	0	0	1

Table.3 Switching states of seven level cascade inverter

The advantages and disadvantages of cascaded H-bridge inverter is as follows:

Advantages:

- 1) The series structure allows a scalable, modularized circuit layout and packaging since each bridge has the same structure.
- 2) Requires the least number of components considering there are no extra clamping diodes or voltage balancing capacitors.
- 3) Switching redundancy for inner voltage levels are possible because the phase voltage output is the sum of each bridges output.

- 4) Potential of electric shock is reduced due to the separate DC sources.

Dis-advantages:

- 1) Limited to certain applications where separate d.c sources are available.

III. CARRIER BASED PWM METHODS

The natural sampling techniques for a multilevel inverter are categorized into two and they are:

- 1. Single-Carrier SPWM (SCSPWM)
- 2. Sub-Harmonic PWM (SHPWM)

Sub-Harmonic PWM is an exclusive control strategy for multilevel inverters and has further classifications. They are

- 1. Carrier Disposition PWM methods
 - i. Phase Disposition (PD)
 - ii. Alternative Phase Opposition Disposition (APOD)
 - iii. Phase Opposition Disposition (POD)

2. Inverted Sine Wave PWM Method

(A) Phase Disposition:

If all carriers are selected with the same phase, the method is known as Phase Disposition (PD) method. It is generally accepted that this method gives rise to the lowest harmonic distortion in higher modulation indices when compared to other disposition methods. This method is also well applicable to cascade inverters. The waveform of carriers of this method is illustrated in Fig 5.

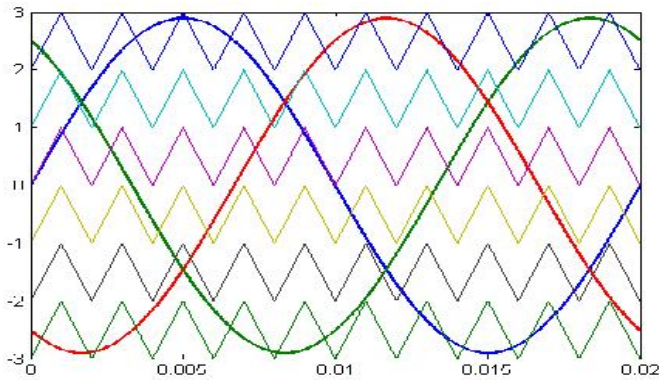
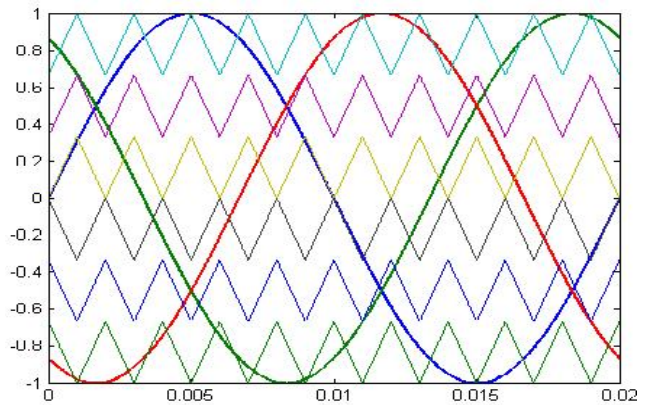


Fig (5) Phase Disposition Input PWM

(B) Phase Opposition Disposition:

The Phase Opposition Disposition (POD) method, having the carriers above the zero line of reference voltage out of phase with those of below this line by 180 degrees as shown in Fig. 5 is one another of the carriers' disposition group. Compared to the PD method, this method has better results from the viewpoint of harmonic performances in lower modulation indices. In POD method, there is no harmonic at the carrier frequency and its multiples and the dispersion of harmonics occurs around them.



Fig(6) POD Input PWM

(C) Alternate Phase Opposition Disposition:

The third member of the carriers' disposition group is known as Alternative Phase Opposition Disposition (APOD) method. Each carrier of this method is phase shifted by 180 degrees from its adjacent one. It should be noted that POD and APOD methods are exactly the same for a 3-level Inverter. This method gives almost the same results as the POD method. The major differences are the larger amount of third order harmonics which is not important because of their cancellation in line voltages. Thus, this method results in a better THD for line voltages when comparing to the POD method. The carrier waveforms of this method are illustrated in Fig 7

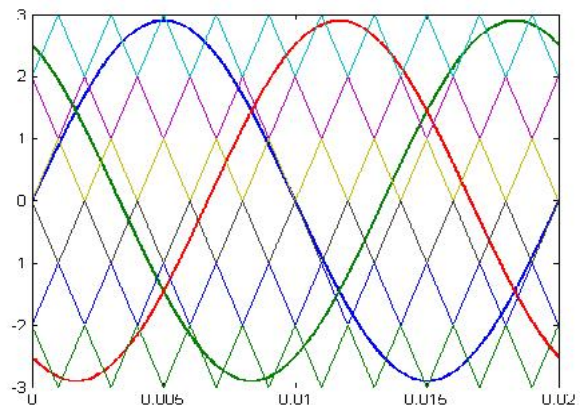


Fig (7) APOD Input PWM

2) Inverted Sine Wave:

The inverted sine carrier PWM (ISPWM) method uses the conventional sinusoidal reference signal and an inverted sine carrier. The control strategy uses the same reference synchronized sinusoidal signal) as the conventional SPWM while the carrier triangle is a modified one. The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation. For an 'm' level inverter, (m-1) carrier waves are required. when the amplitude of the modulating signal is greater than that of the carrier signal. The proposed control strategy has a better spectral quality and a higher fundamental output voltage without any pulse dropping. **Fig.8**

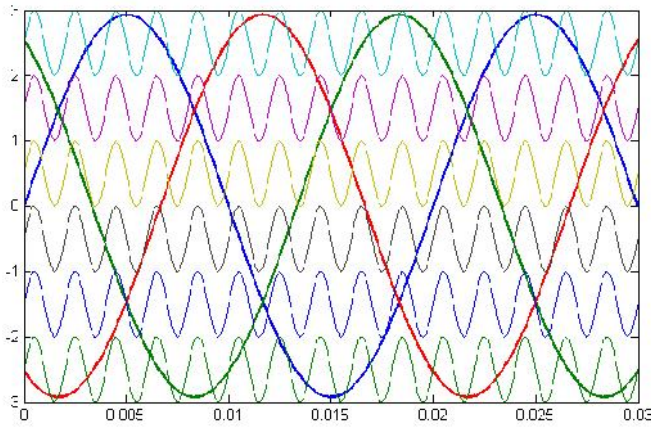


Fig (8) Inverted Sine Wave Input PWM

3. Simulation Results:

(1) PD:

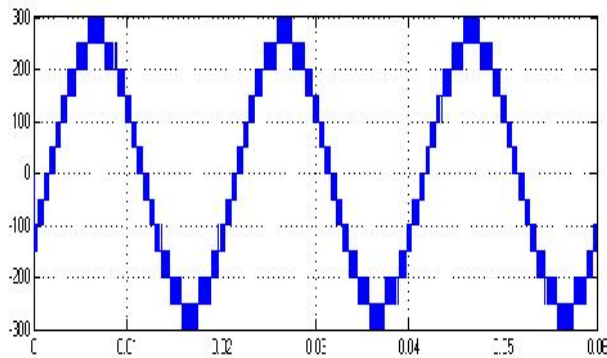


Fig 9 (a)

TOTAL HARMONIC DISTORTION:

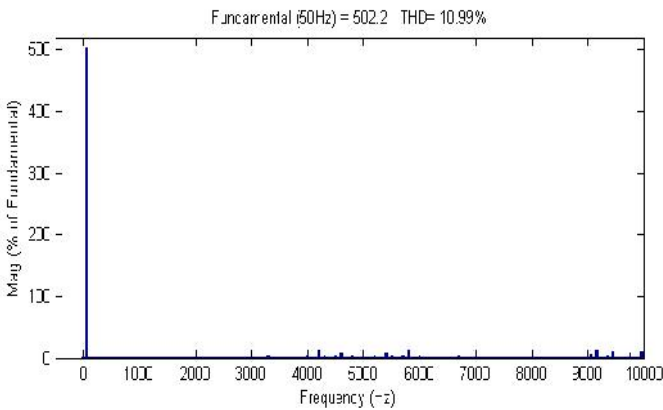


Fig 9 (b)

Fig. 9 (a). Inverter output line voltage and **(b)** corresponding harmonic spectrum of C 7LI

Fig. 9(a) and (b) shows the Inverter output line voltage and THD as 10.40% and Fundamental component of 520.2 Volts for Sub-harmonic PWM based three-phase cascaded seven level inverter.

(2) POD:

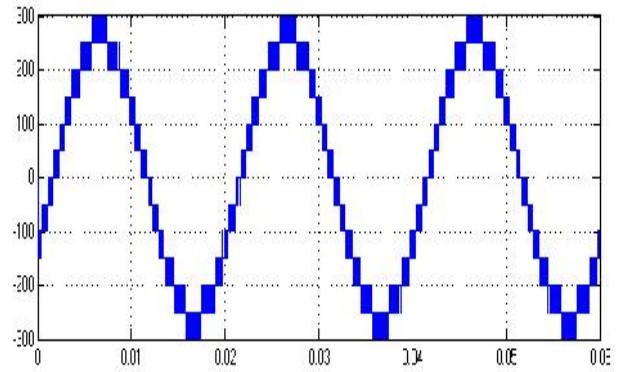


Fig 10 (a)

TOTAL HARMONIC DISTORTION:

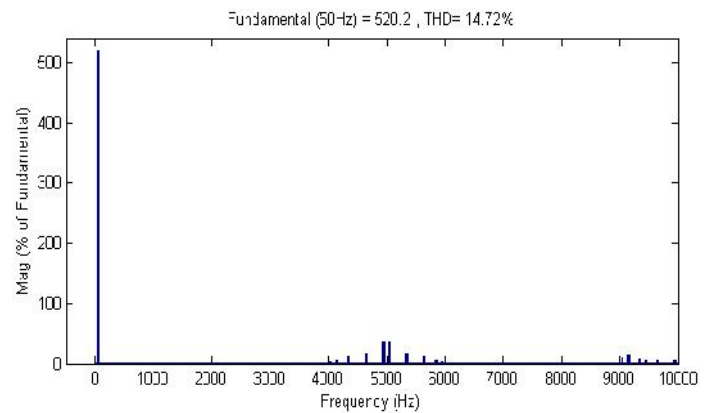


Fig 10 (b)

Fig. 10 (a). Inverter output line voltage and **(b)** . Corresponding harmonic spectrum of C 7LI

Fig. 10(a) and (b) shows the Inverter output line voltage and THD as 14.72% and Fundamental component of 520.2 Volts for modified reference modulated technique based three-phase cascaded seven level inverter.

(3) APOD:

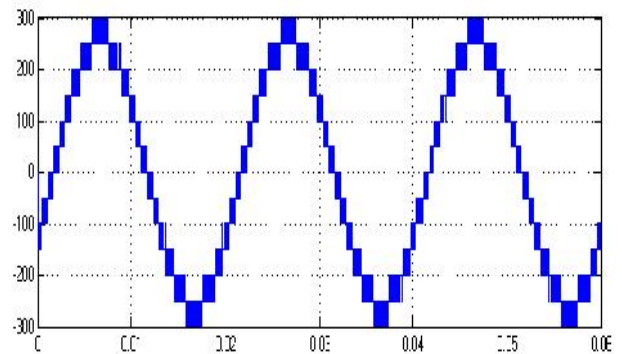


Fig 11 (a)

TOTAL HARMONIC DISTORTION:

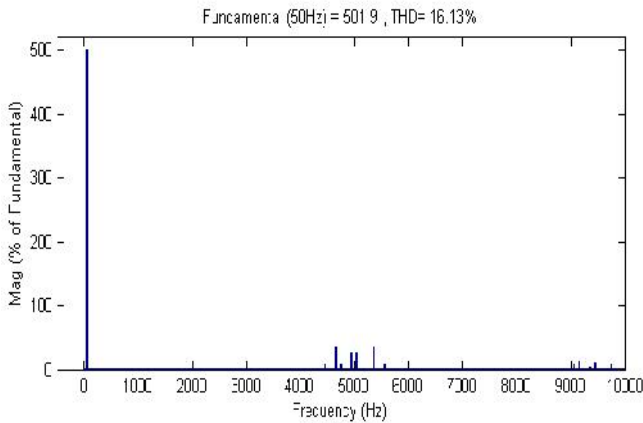


Fig 11 (b)

Fig. 11 (a). Inverter output line voltage and (b) . Corresponding harmonic spectrum of C 7LI

Fig. 11(a) and (b) shows the Inverter output line voltage and THD as 10.20% and Fundamental component of 499.4 Volts for modified reference modulated technique based three-phase cascaded seven level inverter.

(4) INVERTED SINEWAVE:

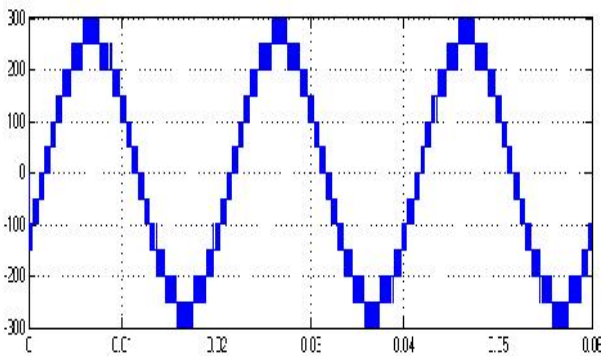


Fig 12 (a)

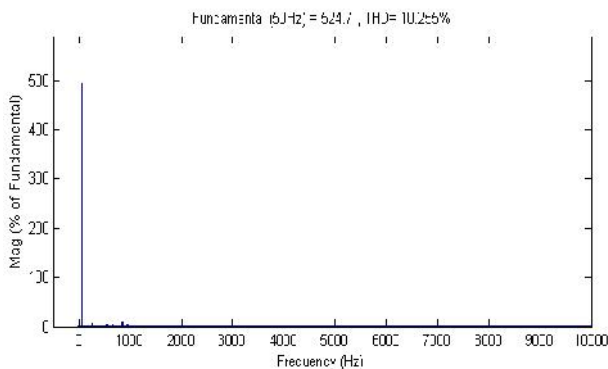


Fig 12 (b)

Fig. 12(a) and (b) shows the Inverter output line voltage and THD as 16.13% and Fundamental component of 501.9 Volts for modified reference modulated technique based three-phase cascaded seven level inverter

3.3 Comparison of Results for proposed PWM Methods

PWM technique	Input Voltage (volts)	Fundamental output voltage(volts)	Switching frequency (hertz)	THD (%)
PD	300	520.2	5000	10.40
POD	300	520.2	5000	14.72
APOD	300	501.9	5000	16.13
Inverted SINE	300	524.7	5000	10.25

Table 4 : Comparison of THD for various PWM Methods

4. Conclusion

The Cascaded three-phase seven level inverter is simulated for different PWM methods. The simulation results with harmonic spectrum are presented, and in this presentation it is concluded that inverted sine wave PWM technique has given good harmonic spectrum (10.25%) and fundamental output Voltage (524.7V) when compared with existing PWM techniques.

5. References

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