

# Design and Analysis of Soft Switched PWM Full Bridge DC–DC Converter for Regulated Voltage

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**Abstract**— In this paper, The new soft switched full bridge converter associated with a nondissipated snubber operates using phase-shift control and coupled output inductor to reduce the circulating current in primary and the voltage stress in the secondary side, this results in reduced conduction losses and switching frequency their by regulated output voltage is achieved. The proposed converter is analyzed using MATLAB/Simulink software.

**Keywords**— Full bridge converter, regulated output voltage, soft switch.

## I. INTRODUCTION

Switch-mode power supplies are employed in dc voltage step-up or step-down, as several dc-dc converters can be used for this purpose. Soft switching PWM topologies [3, 4, 5,6] have advantages such as low switching losses, Constant frequency of operation and simple control, However they have load limitation and high current or voltage ratings for semiconductor devices.

The full-bridge converter is widely used in medium-to-high Power dc–dc conversions because it can achieve Soft-switching without adding any auxiliary switches. The phase-shift full-bridge (PSFB) topology is one of the most popular choices when dealing with isolated dc-dc conversion, mainly due to its high efficiency and low electromagnetic interference (EMI) [11]. However, the circulating loss in primary is high for a conventional PSFB converter especially in high input current application. Soft switching techniques have been proposed for PWM full bridge converter and can be classified into two types: one is zero-voltage-switching (ZVS) [12] and the other is zero voltage and zero-current-switching (ZVZCS) [13]. In ZVZCS PWM full-bridge converters, one leg achieves ZVS, and the other leg achieves ZCS [14].

A dc-dc full-bridge converter using the no dissipative snubber presented in [15] has proven to be adequate. This topology also develops some prominent advantages, since soft switching is achieved for a wide load range and conduction losses are almost the same as those in the hard-switched converter. This paper proposes a dc-dc full-bridge topology with soft switching of the controlled semiconductor switches to achieve regulated output voltage.

This paper is organized as follows: Section II shows the block diagram of proposed full bridge converter. Section III describes the operating modes of proposed converter. Section IV shows the designing procedure of proposed converter. Section V presents the simulation and results of proposed converter. Section VI is conclusion.

## II. DC-DC FULL-BRIDGE CONVERTER

Fig. 1 shows the block diagram of full-bridge converter associated with a non-dissipative snubber. This topology employs a coupled output inductor to minimize the currents through the primary winding and the main switches, resulting in reduced conduction losses and high switching frequency. The snubber cell introduced here is an adaptation of the structure presented in [15].

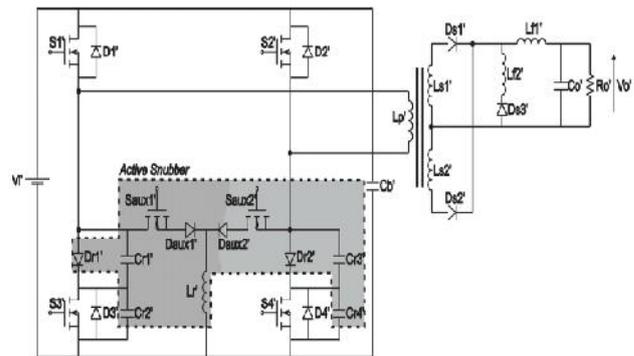


Fig. 1 Full bridge soft switched dc-dc converter with non-dissipative snubber.

## III. OPERATING PRINCIPLE

In order to study the proposed topology, the operation of the converter shown in Fig. 1 is divided in eight stages shown in Fig(2) to Fig.(9). A single part is considered in the analysis due to the inherent symmetry of the circuit. The main waveforms are shown in Fig. 10.

The analysis is based on the following assumptions:

- all switches and diodes are ideal;
- the input voltage  $V_i$  is equal to the output voltage of the interleaved boost converter, represented by  $V_0$ ;
- the voltage across capacitor  $C_b$  is considered constant and ripple-free;
- the input current  $I_i$  is constant and flows through capacitor  $C_b$ .

**First Stage ( $t_0, t_1$ ):** Switches  $S_1$  and  $S_4$  are turned on at the beginning of the stage. The voltage across the primary winding is equal to that across capacitor  $C_b$  ( $V_{Cb}$ ). There is power transfer from the primary side to the secondary side. The stage finishes when switch  $S_4$  is turned off.

The voltage across inductor  $L_{f1}$  is:

$$V_{Lf1}(t) = \frac{V_i}{n} V_0 \quad (1)$$

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Consequently the voltages across the secondary windings of the transformer can be obtained as:

$$V_{s1}(t) = V_{s2}(t) = V_{Lfl}(t) + V_0 \quad (2)$$

The time interval that corresponds to this stage is:

$$\Delta t_1' = t_1' - t_0' = \frac{\alpha' n L_{fl}' \sqrt{C_r'}}{1 - n \frac{V_0'}{V_1'}} \quad (3)$$

**Second Stage ( $t_1', t_2'$ ):** This stage begins when switch  $S_4'$  is turned off. Capacitors  $C_{r4}'$  is charged to the input voltage, until diode  $D_{r2}'$  is reverse biased.

The voltage across inductor  $L_{fl}'$  is:

$$V_{Lfl}'(t) = \frac{1}{n} \left[ -\frac{I_i'}{C_{r4}' \omega_0'} \sin(\omega_0' t) + V_i' \cos(\omega_0' t) \right] - V_0' \quad (4)$$

$$i_{Lr}'(t) = \frac{V_i'}{L_r'} t \quad (5)$$

The time interval that corresponds to this stage is:

$$\Delta t_4' = t_4' - t_3' = \frac{\alpha'}{K_1' \omega_0'} \quad (6)$$

**Fifth Stage ( $t_4', t_5'$ ):** This stage begins when switch  $S_1'$  is turned off in zero voltage condition, because the current through  $L_r'$  equals  $I_i'$ . At the same time, there is resonance between  $L_r', C_{r1}'$ , and  $C_{r2}'$ . The voltages across capacitors  $C_{r1}'$  and  $C_{r2}'$  are  $-V_{Cr1}'$  and null, respectively. Switch  $S_3'$  is then turned on in zero voltage condition.

The time interval that corresponds to this stage is:

$$\Delta T_2' = t_2' - t_1' = \frac{1}{\omega_0'} \sqrt{\frac{L_p'}{L_r'}} \left( \frac{x'+1}{x'} \right) \tan^{-1} \left[ \frac{K_2'}{\alpha'} \right] \quad (7)$$

**Third Stage ( $t_2', t_3'$ ):** The current is freewheeling through the primary winding, as switch  $S_2'$  can be turned on in zero voltage condition, since the current flows through  $D_2'$ . The voltage across coupled inductor  $L_{f2}'$  causes the current through the primary winding to decrease quickly until it becomes null, as the current through  $L_{f2}'$  becomes maximum. This stage is responsible for phase shift control, and it finishes when  $S_{aux1}'$  is turned on in zero current condition due to inductor  $L_r'$ . The voltages across  $C_{r1}'$  and  $C_{r2}'$  are equal to null and  $V_i'$ , respectively.

The voltages across inductors  $L_{f1}'$  and  $L_{f2}'$  are:

$$V_{Lfl}' = \frac{L_{f1}'}{L_{f2}' - L_{f1}'} V_0' \quad (8)$$

$$V_{Lf2}' = \frac{L_{f2}'}{L_{f1}' - L_{f2}'} V_0' \quad (9)$$

The time interval that corresponds to this stage is:

$$\Delta t_3' = \quad (10)$$

$$\frac{T_s'}{2} - (\Delta t_1' + \Delta t_2' + \Delta t_4' + \Delta t_5' + \Delta t_6' + \Delta t_7' + \Delta t_8')$$

**Fourth Stage ( $t_3', t_4'$ ):** Switches  $S_2'$  and  $S_{aux1}'$  are turned in zero current condition. The current through  $L_r'$  increases

linearly until it reaches  $I_i'$ . This stage finishes when switch  $S_1'$  is turned off in zero voltage condition.

The current through resonant inductor  $L_r'$  is:

The voltages across resonant capacitors  $C_{r1}'$ , and  $C_{r2}'$  are:

$$V_{Cr1}'(t) = -\frac{I_0'}{\alpha'(X'+1)} \sqrt{\frac{L_r'}{C_r'}} [1 - \cos(\omega_0' t)] \quad (11)$$

$$V_{Cr2}'(t) = -\frac{I_0' X'}{\alpha'(X'+1)} \sqrt{\frac{L_r'}{C_r'}} [1 - \cos(\omega_0' t)] + V_i' \quad (12)$$

The time interval that corresponds to this stage is:

$$\Delta t_5' = t_5' - t_4' = \frac{1}{\omega_0'} \cos^{-1} \frac{2X'+1}{X'} \quad (13)$$

**Sixth Stage ( $t_5', t_6'$ ):** Capacitor  $C_{r2}'$  remains discharged. There is a resonance between  $L_r'$  and  $C_{r1}'$ . Then auxiliary switch  $S_{aux1}'$  can be turned off in zero current condition. The stage finishes when the current through  $L_r'$  becomes null. The current through resonant inductor  $L_r'$  is:

$$i_{Lr}(t)' = I_i' - \frac{V_i'}{X'} \sqrt{\frac{C_r'(X'+1)}{L_r'}} \sin(\omega_0' t) \quad (14)$$

The voltage across resonant capacitor  $C_{r1}'$  is:

$$V_{Cr1}'(t) = -\frac{V_i'}{X'} \cos(\omega_0' t) \quad (15)$$

The time interval that corresponds to this stage is:

$$\Delta t_6' = t_6' - t_5' = \frac{\sqrt{X'+1}}{\omega_0'} \sin^{-1} \left[ \frac{\alpha' X'}{K_1' \sqrt{X'+1}} \right] \quad (16)$$

**Seventh Stage ( $t_6', t_7'$ ):** The current through  $L_r'$  becomes null. Capacitor  $C_{r1}'$  is fully discharged linearly.

The voltage across resonant capacitor  $C_{r1}'$  is:

$$V_{Cr1}'(t) = \frac{I_i'}{C_r'(X'+1)} t - \frac{V_i'}{X'} \quad (17)$$

The time interval that corresponds to this stage is:

$$\Delta t_7' = t_7' - t_6' = \frac{K_1' X'+1}{\alpha' \omega_0' X'} \quad (18)$$

**Eighth Stage ( $t_7', t_8'$ ):** The voltage across  $C_{r1}'$  becomes null, as switches  $S_1'$  and  $S_3'$  are turned on and off simultaneously, respectively, and a new switching cycle begins. During this stage, there is power transfer to the load.

The time interval that corresponds to this stage is:

$$\Delta t_8' = t_8' - t_7' = D' T_s' - \left[ \frac{\sqrt{X'+1}}{\omega_0'} \sin^{-1} \left[ \frac{\alpha' X'}{K_1' \sqrt{X'+1}} \right] + \frac{K_1'(X'+1)}{\alpha' X' \omega_0'} \right] \quad (19)$$

where  $D'$  is the duty cycle of switch  $S_1'$ .

By definition, the following expressions result:

$$C_r' = \frac{C_{r1}' C_{r2}'}{C_{r1}' + C_{r2}'} \quad (20)$$

$$X' = \frac{C_{r1}'}{C_{r2}'} \tag{21}$$

$$C_{r1}' = C_r'(X' + 1) \tag{22}$$

$$C_{r2}' = \frac{C_r'(X' + 1)}{X'} \tag{23}$$

$$\omega_0' = \frac{1}{\sqrt{L_r' C_r'}} \tag{24}$$

$$\omega_{0p}' = \frac{1}{\sqrt{L_p' C_{r4}'}} \tag{25}$$

$$\omega_{01}' = \frac{1}{\sqrt{L_r' C_{r1}'}} \tag{26}$$

$$\alpha' = \frac{I_0'}{V_1'} \sqrt{\frac{L_r'}{C_r'}} \tag{27}$$

$$n_1 = n_2 = n \tag{28}$$

$$C_{r1}' = C_{r3}' \tag{29}$$

$$C_{r2}' = C_{r4}' \tag{30}$$

$$K_1' = \frac{I_0'}{I_1'} \tag{31}$$

$$K_2' = K_1' \sqrt{\frac{L_r'(X' + 1)}{L_p' X'}} \tag{32}$$

$$K_3' = \frac{I_{mag}'}{I_1'} \tag{33}$$

$$K_{lf}' = \frac{L_{f1}'}{L_{f2}'} \tag{34}$$

$$f_s' = \frac{1}{T_s'} \tag{35}$$

$$K_f' = \frac{f_s'}{f_0'} \tag{36}$$

where:

$\omega_0', \omega_{01}', \omega_{0p}'$  – resonance frequencies [rad/s];

$\alpha'$  – normalized load current [A];

$L_p'$  – primary inductance [H];

$f_s'$  – switching frequency [Hz];

$V_i'$  – input voltage [V];

$I_i'$  – input current [A];

$T_s'$  – switching period [s];

$I_{mag}'$  – magnetizing current [A];

$n=n_1=n_2$  – turns ratio.

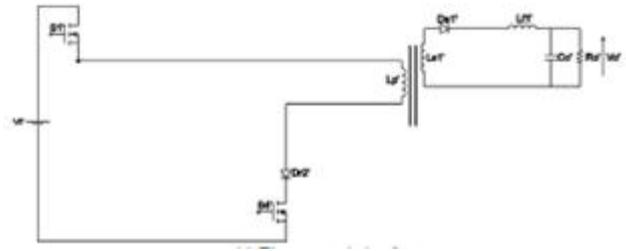


Fig.2 First Stage

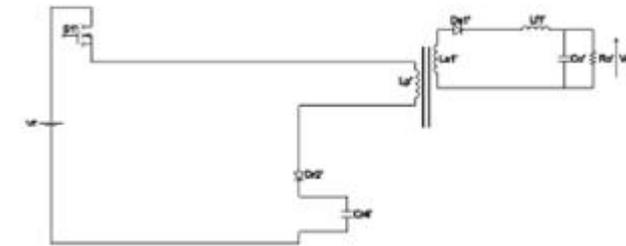


Fig.3 Second Stage

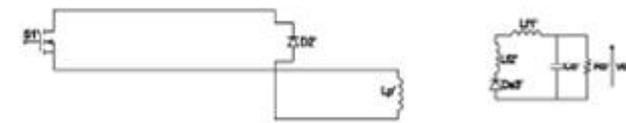


Fig.4 Third Stage

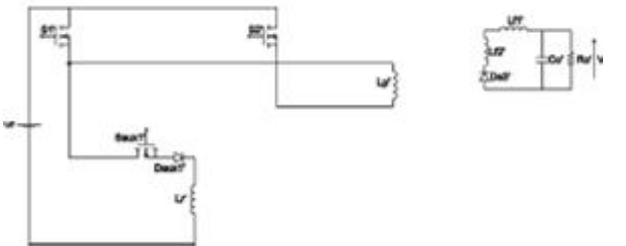


Fig.5 Fourth Stage

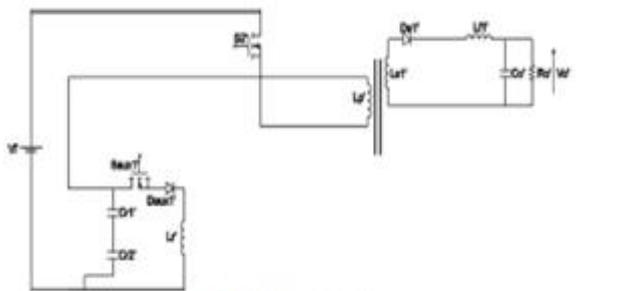


Fig.6 Fifth Stage

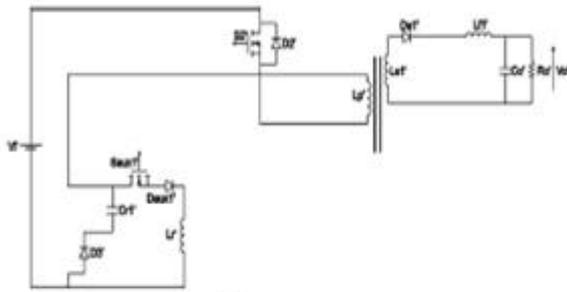


Fig.7Sixth Stage

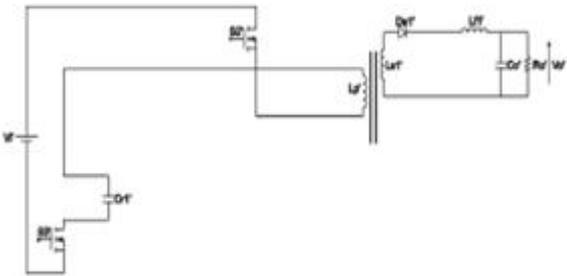


Fig.8 Seventh Stage

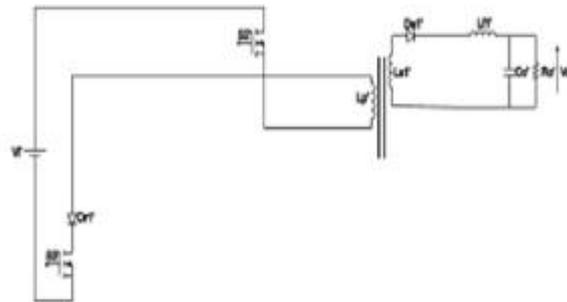


Fig.9 Eight Stage

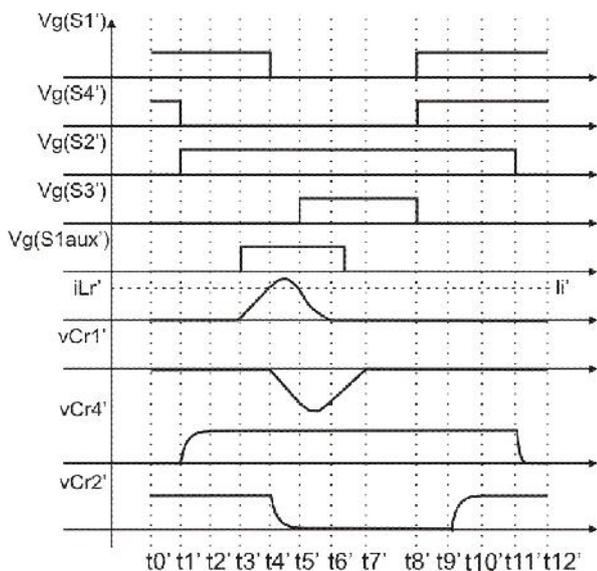


Fig.10 operating waveforms

IV. DESIGN PROCEDURE

This section presents a design procedure for the full-bridge converter, whose specifications are given in Table I.

TABLE I  
FULL-BRIDGE CONVERTER SPECIFICATIONS

Parameter	Value
DC input voltage	$V_i'=V_o=400$ V
Output power	$P_o'=1.5$ kW
DC output voltage	$V_o'=60$ V
Switching frequency	$f_s'=100$ kHz

The resonance frequency  $f_0'$  must be greater than the switching frequency  $f_s'$ :

$$f_0' = \frac{f_s'}{0.083} = \frac{100 \cdot 10^3}{0.083} = 1.2 \text{ MHz} \tag{37}$$

The design of the resonant elements is related to (78). Then expression (36) can be written as:

$$\omega_0' = \frac{1}{\sqrt{L_r' C_r'}} = 2\pi f_0' \tag{38}$$

Substituting (78) in (79) gives:

$$L_r' C_r' = 1.76 \cdot 10^{-14} \tag{39}$$

Analogously, expression (39) can be rearranged as:

$$\frac{L_r'}{C_r'} = \left[ \frac{\alpha' V_i'}{I_0} \right]^2 \tag{40}$$

$$I_0' = \frac{P_o'}{V_o'} = \frac{1500}{60} = 25 \text{ A} \tag{41}$$

$$\frac{L_r'}{C_r'} = 3136 \tag{42}$$

Solving the equation system represented by (41) and (42) gives  $L_r'$  and  $C_r'$  as:

$$\begin{aligned} L_r' &= 7.43 \mu\text{H} \\ C_r' &= 2.37 \text{ nF} \end{aligned} \tag{43}$$

If  $C_r'=2.37$  nF and  $C_{r2}'=7.5$  nF are substituted in (32), one can determined  $C_{r1}'=3.44$  nF, although  $C_{r1}'=3.3$  nF can be chosen.

V. SIMULATION AND RESULTS

Matlab/Simulink block diagram of the full bridge converter was implemented using the parameters set shown in Table II. Simulink model of converter is shown in fig.(11) without step change in load and with change in step load is shown in Fig.(12). Results of proposed converter are shown in Fig.(13) to Fig.(19).

TABLE II  
FULL-BRIDGE CONVERTER PARAMETERS

Parameter	Value
Resonant inductor	$L_r'=7.43 \mu\text{H}$
Resonant capacitors	$C_{r1}'=C_{r3}'=3.3 \text{ nF}$ $C_{r2}'=C_{r4}'=7.5 \text{ nF}$
Primary turns	$N_p=15$
Secondary turns	$N_{s1}=N_{s2}=5$
Bulk capacitor	$C_b'=300 \mu\text{H}$
Output filter inductor	$L_{f1}'=75 \mu\text{H}$
Coupled inductor	$L_{f2}'=25 \mu\text{H}$
Output filter capacitors	$C_o'=25 \mu\text{F}$

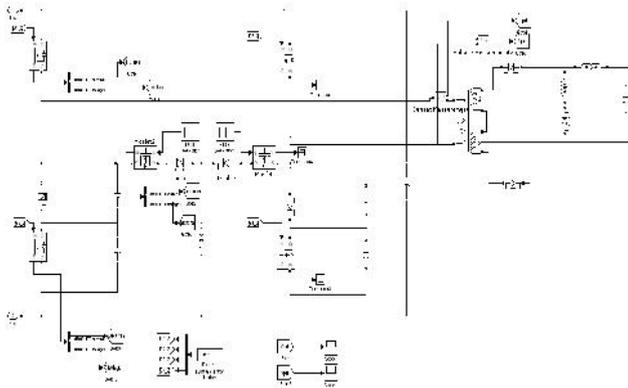


Fig.11 MATLAB/Simulink model of full bridge converter

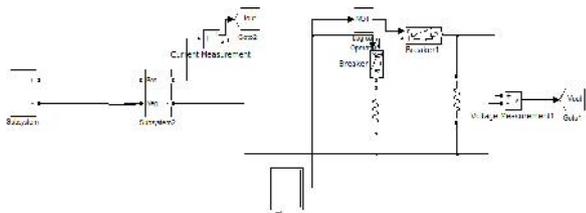


Fig.12 MATLAB/Simulink model of full bridge converter with step change in load

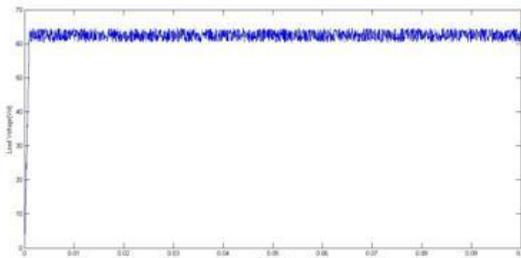


Fig.13 Output voltage without step change in load

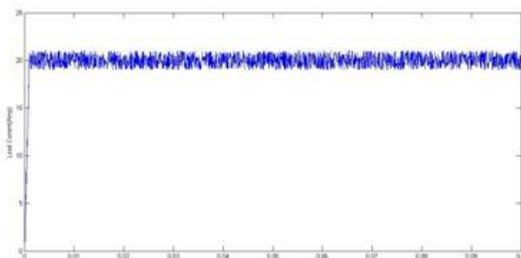


Fig.14 Load Current without step change in load

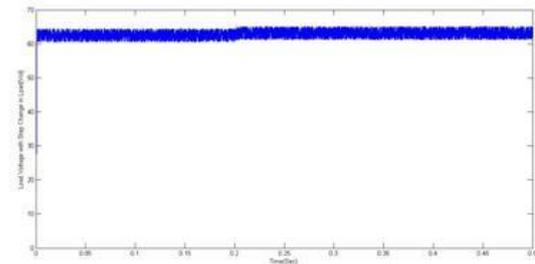


Fig.15 Output voltage with step change of load at 0.25 sec.

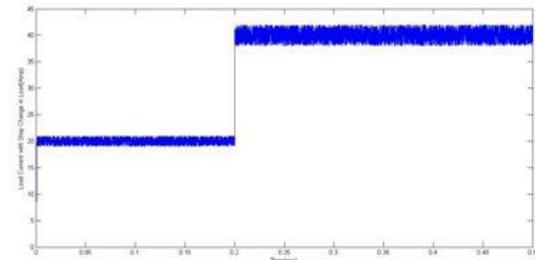


Fig.16 Load Current with step change of load at 0.25 sec.

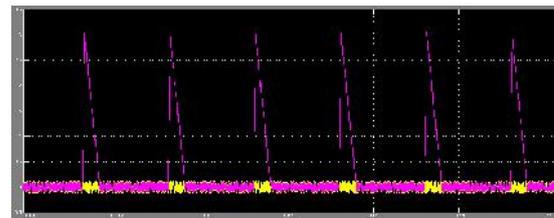


Fig.17 Voltage and Current waveform of switch S1

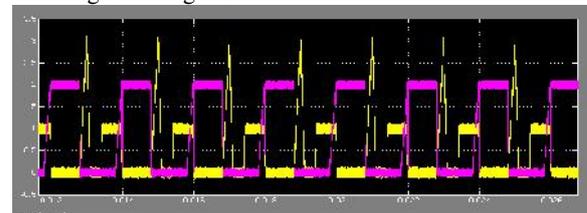


Fig.18 Voltage and Current waveform of Saux1

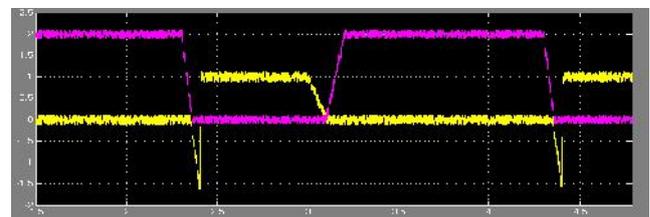


Fig.19 Voltage and Current waveform of switch S3

## VI. CONCLUSIONS

A PWM full-bridge converter is proposed in this paper, it employs an active snubber with soft switching technique reduces the conduction losses, hence conversion efficiency can be increased. In the meanwhile reduced filter capacitance

compared with the traditional full bridge converter. The operation principle features and comparisons are illustrated. Simulation results show the performance of the converter.

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