A Low Power and High Performance ON-Chip Interconnect Using Current Mode Signalling Scheme

Prabakaran J and Ravi V

***Abstract*— Current-Mode Signalling (CMS) with bias scheme is one of the most promising scheme for high-speed low power communication over long on-chip interconnects. The proposed CMS scheme and a competing CMS scheme (CMS-Fb) are fabricated in 180-nm CMOS technology. When using current mode signalling for on chip interconnects, we obtain a significant improvement in both speed and power consumption. It consumes much less power compared to the current mode signalling feedback scheme. Also current mode signalling derives its advantages over voltage mode due to the reduced swing on the line. By using ring oscillator, buffer, D-latch as a delay element in current mode signalling bias scheme we can reduce the power consumption, delay for on chip interconnect signal transition. Dynamic overdriving method used to improve the performance of current mode signalling bias scheme. That is, current mode transmission can be speeded up by using high drive current. However, this increases static power consumption. One possible solution is to dump high drive current only when the state of the line needs to be changed from 0 to 1 or from 1 to 0. When the line remains at 1 or 0 from one bit to the next, here use a small drive current to maintain the line at the required voltage.**

***Index Terms*— Current-mode Signalling (CMS) , Current-mode Signalling feedback scheme(CMS-Fb) , Current-mode Signalling bias scheme(CMS-Bias) , Dynamic overdriving**

I. INTRODUCTION

Speed and power consumption of on-chip interconnect network have become important in advanced CMOS technologies .It is difficult to meet desired power and performance specifications of modern system-on-chips (SoCs) and multicore processors with buffer inserted long interconnects [2].Many alternate repeater circuits and signalling schemes have been suggested in recent past to achieve high-speed low-power communication over long on-chip interconnects [3] [17]. In modern CMOS technologies, process variations cause significant variations in device parameters which can lead to performance degradation of these signalling techniques. Hence, a signalling scheme for on-chip interconnects is also required to be robust against parameter variations.

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We first review the most promising signalling schemes for energy-efficient communication over long wires. Current-mode signalling (CMS) scheme has the potential to improve both speed and dynamic power consumption. It consumes much less power compared to the improved repeater circuits (such as self-timed repeaters [16] and boosters [10]) and signalling schemes such as near-speed of light communication [1] and transition-aware signalling [7]. Current-mode signalling can be used to provide higher interconnect bandwidth when compared to traditional full-swing voltage-mode signalling, at the expense of increased DC power dissipation. Current-mode signalling is easier to implement with driver pre-emphasis technique because its logic states are determined by current values instead of voltage levels.

Current mode signalling derives its advantages over voltage mode due to the reduced swing on the line. Careful design is necessary otherwise small changes in device parameters can have a disproportionate effect on the performance of the system.The proposed dynamic overdriving CMS scheme that is robust improvement in delay, energy and EDP over voltage-mode schemes for a wide range of line lengths, data rates and data activity factors. The proposed scheme employs a smart bias circuit in the transmitter which makes it robust against inter-die variations. The operation of the circuit does not rely on matching of the transistor parameters of the transmitter and the receiver. Current mode transmission offers the possibility for improving Latency, Throughput and Power.

II. CMS WITH BIAS SCHEME

The proposed CMS-bias scheme consists of transmitter and receiver part . The proposed transmitter employs two drivers [8] (a strong driver and a weak driver) with NAND and NOR gates like the transmitter of CMS-Fb scheme. In the proposed transmitter, duration for which the strong driver is turned on is controlled by a delay element. The strong and weak drivers employ single transistor current sources.

The bias voltages of these current sources are generated from a specially designed bias circuit such that current through strong and weak driver remain constant across all process corners. The proposed receiver uses a diode connected pMOS and nMOS (terminating inverter) followed by an inverter chain. The terminator inverter holds the line voltage near its switching threshold. Inverter

amplifier (IA) and subsequent inverters amplify the small line voltage swing to digital logic levels.

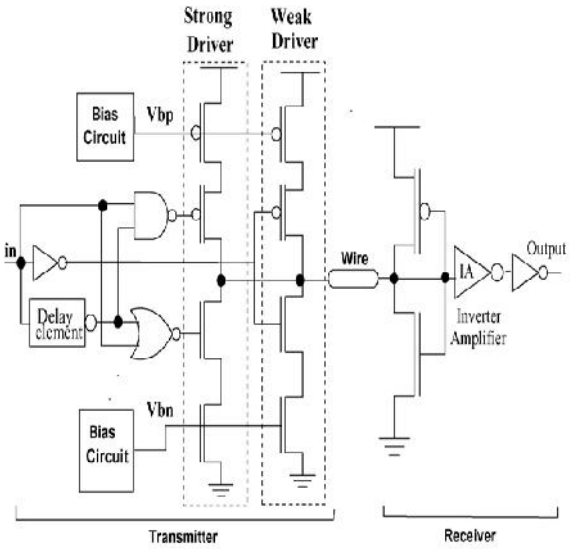

Figure 1 CMS with bias scheme[9]

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The bias voltages Vbp, Vbn from the bias circuits is given as input to the strong driver, weak driver. The duration for the strong driver turned on is controlled by the delay element. In weak driver when the input is 1, the p channel driver gate is low. This charges up the output. When the input is 0 the n channel driver transistor is enabled by a high level at its gate. The transistor discharges the line. In strong driver the P channel gate is low (enabled) only when both inputs to the NAND are 1. The N channel gate is high (enabled) only when both inputs to the NOR gate are 0.

A. WEAK DRIVER

The weak driver provides the minimal drive required to keep the line (terminated by low impedance) at the desired voltage level. When the input is 1, the p channel driver gate is low (enabled). This charges up the output. As the line voltage reaches VDD − VTp, the upper p-channel transistor turns off, restricting line voltage swing in the up direction.

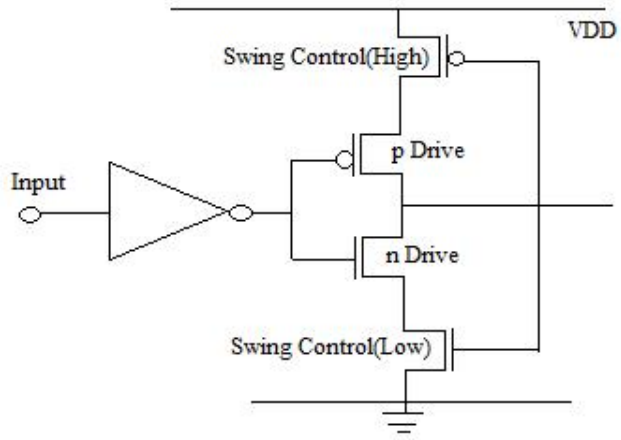

Figure 2 Weak driver[9]

Similarly when the input is 0 the n channel driver transistor is enabled by a high level at its gate. The transistor discharges the line. However, when the line voltage approaches VTn during discharge, the lower transistor turns off, stopping the discharging process. Thus the line can only swing between VDD − VTp and VTn.

B. STRONG DRIVER

The strong driver should be enabled only when the input and the level on the output line do not represent the same logic.

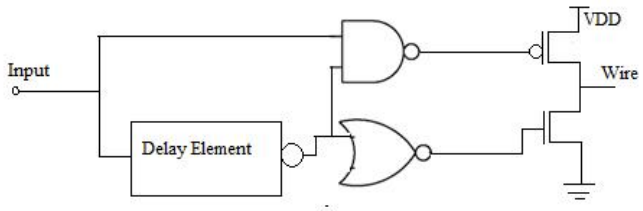

Figure 3 Strong driver[9]

The P channel gate is low (enabled) only when both inputs to the NAND are 1. This will happen only when the input is high AND the line is at 0. This is indeed the condition when we want the strong driver to charge the line. The N channel gate is high (enabled) only when both inputs to the NOR gate are 0. This will happen only when the input is low AND the line is at 1.Notice that the input to the feedback inverter is a low swing level around VDD/2. Therefore it consumes static power.

The action of the strong driver is self-limiting. This is because both NAND and NOR receive the input and the inverted logic level of the line. If the input and the logic level of the line are the same, NAND and NOR are fed with input and input. Thus one of the inputs to NAND/NOR is 1, while the other is 0. This ensures that the output of NAND is 1, while that of NOR is 0, so that both the p and n channel

transistors are OFF.Therefore the strong driver does not need a series transistor as was the case for the weak driver. When the Input = 1 and Wire voltage < Vm, the inverter output = 1, NAND output = 0 and NOR output = 0.The P channel driver is ON and dumps current to charge the line. When the Input = 0 and Wire voltage > Vm, the inverter output = 0, NAND output = 1 and NOR output = 1.the N channel driver is ON and sinks current to discharge the line. As soon as low swing logic level on the line becomes equal to the logic level at the input Inverter output = input, and so NAND output = 1, NOR output = 0; which disables both drive transistors automatically.

C. DYNAMIC OVER DRIVING (Pre-Emphasis)

Current mode transmission can be speeded up by using high drive current. However, this increases static power consumption. One possible solution is to dump high drive current only when the state of the line needs to be changed from 0 to 1 or from 1 to 0. When the line remains at 1 or at 0 from one bit to the next, we use a small drive current to maintain the line at the required voltage. This is called Dynamic over Driving. Dynamic Overdriving essentially means amplifying high frequency components of the input signal. Dynamic overdriving used to improve the performance of current mode signalling.

D. BIAS CIRCUIT

The figure4 illustrate bias circuit, which is used in the proposed cms- bias scheme The proposed bias circuit is derived from the conventional resistor based bias circuit. In the ideal resistance based circuit, the pMOS bias voltage increases/decreases from its value defined in the nominal process corner when the pMOS (MP0) becomes fast/ slow due to process variations. As a result, does not change much with process variations. Similarly, changes such that the variations in are less. However, the on-chip resistors can vary by 15% .Hence, in practice, the bias voltages and change not only due to variations in the pMOS and nMOS transistors but also due to variations in the resistance. In this circuit there exists a direct trade-off between area of a resistor and power consumption. Essentially, in the bias circuit the variations in the load device must be much less compared to the variations in the sensor device [pMOS and nMOS].One possible alternative is to employ a long channel transistor as load and Long channel transistors are less susceptible to process variations. The supply voltage Vbn, Vbp are generated by bias circuit.

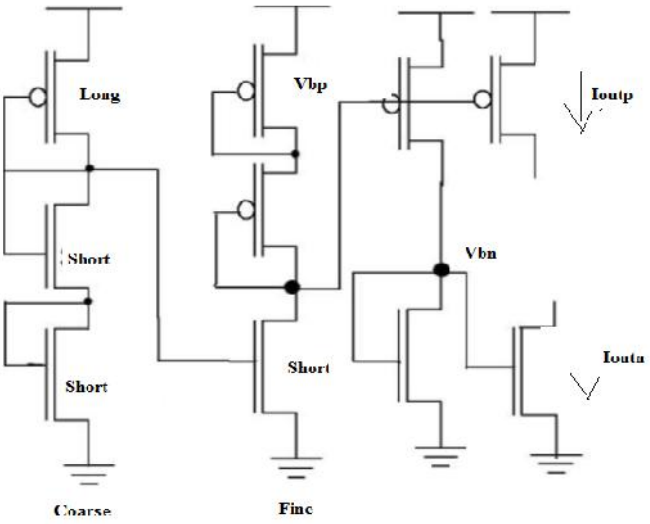

Figure 4 Bias circuit[9]

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III. DELAY ELEMENT

In the proposed transmitter, duration for which the strong driver is turned on is controlled by a delay element. In this proposed scheme using there are three types of delay element. That is ring oscillator, buffer, and d-latch. Take simulation for each delay element and calculate the power consumption, delay, area.

A. RING OSCILLATOR

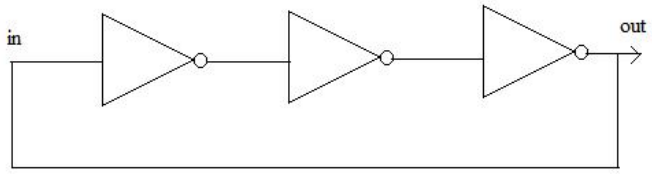

Figure 5 Ring oscillator

A ring oscillator is a device composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing true and false. The NOT gates, or inverters, are attached in a chain the output of the last inverter is fed back into the first. Because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input. This final output is asserted a finite amount of time after the first input is asserted; the feedback of this last output to the input causes oscillation. A circular chain composed of an even number of inverters cannot be used as a ring oscillator; the last output in this case is the same as the input.

The ring oscillator is a distributed version of the delay oscillator. The ring oscillator uses an odd number of inverters to give the effect of a single inverting amplifier with a gain of greater than one. Each inverter contributes to the delay of the signal around the ring of inverters, hence the name ring oscillator. Adding pairs of inverters to the ring increases the total delay and thereby decreases the oscillator frequency.

B. BUFFER

Buffer is a temporary storage element. Buffer insertion is the most widely used method to control interconnect delay. It is inserted into long on chip interconnect into shorter section to reduce propagation delay. Global Interconnect delay can be the determining factor for the speed of an integrated system. We define some critical wire length and when a wire segment exceeds this length, we insert a buffer.

C. D-LATCH

D-latch is a level Triggering device while D Flip Flop is an Edge triggering device. The disadvantage of the D FF is its circuit size, which is about twice as large as that of a D latch. That's why, delay and power consumption in Flip flop is more as compared to D latch. When a circuit is edge triggered the output can change only on the rising or falling edge of the clock. But in the case of level-clocked, the output can change when the clock is high (or low).In edge triggering output can change only at one instant during the lock cycle; with level clocking output can change during an entire half cycle of the clock.

The similarity between latch and flip flop is that the outputs of both depend not only on the current input but also on previous inputs and outputs. A latch does not have a clock signal but flip-flops got clock signal.it is one of the inputs to the flip flop.

IV. EXPERIMENTATION RESULTS

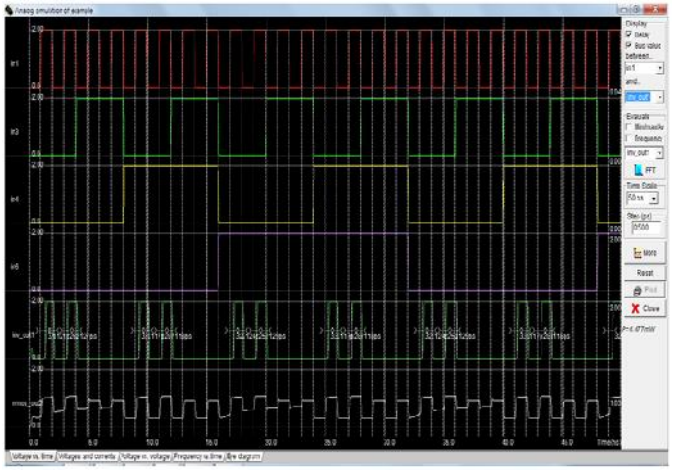

Figure 6 Waveform for CMS-bias with Ring oscillator as a delay element

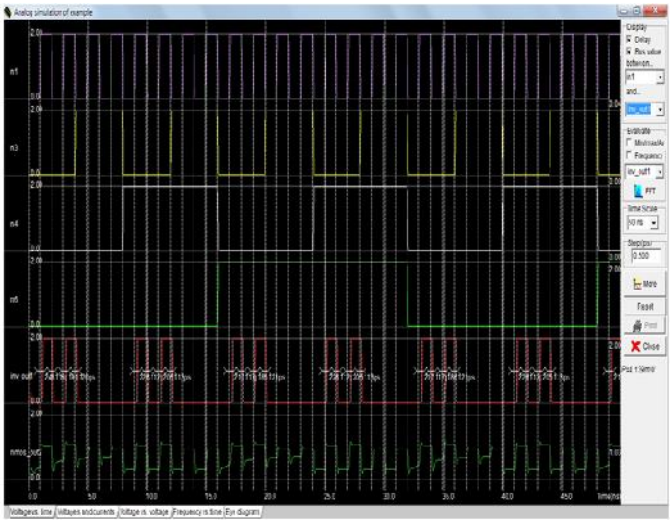

Figure 7 Waveform for CMS-bias with Buffer as a delay element

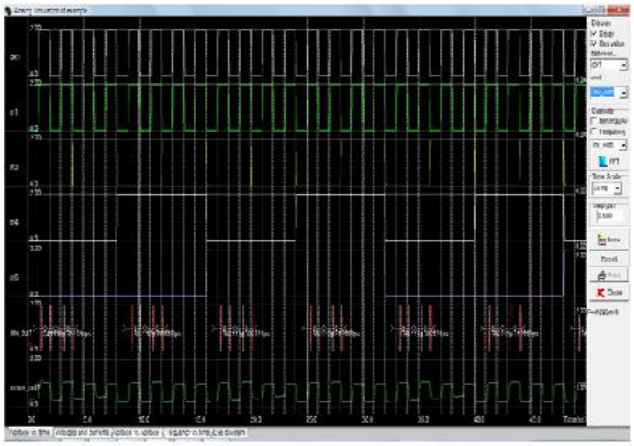

Figure 8 Waveform for CMS-bias with d-latch as a delay element

Figure 6 shows the output waveform for the CMS-Bias scheme using ring oscillator as a delay element. By using this ring oscillator as a delay element we can reduce the area but it consume more power, delay also more compare than the other two delay element. Figure 7 shows the output waveform for the CMS-Bias scheme using buffer as a delay element. By using this buffer as a delay element we can reduce the delay but it consume more power, area also more compare than the other two delay element. Figure 8 shows the output waveform for the CMS-Bias scheme using D-Latch as a delay element. By using this D-Latch as a delay element we can reduce the power consumption but it's area occupation, delay are more compare than the other two delay element.

A. PERFORMANCE OF CMS-BIAS SCHEME

Table 1
Simulation result

Cmos Technology (nm)	Delay Element	Voltage (v)	Power Consumption (mw)	Delay (ns)	Area $(\mu m)^2$
180	Ring oscillator	2	4.477	1.121	111.8× 20.6
180	Buffer	2	4.139	1.093	115.8× 20.6
180	D-Latch	2	4.089	1.107	115.8× 21.6

Three types of delay element used in this current mode signalling bias scheme for reduce the power consumption and also improve the signal transmission speed over long on-chip interconnect. The delay elements are ring oscillator, buffer, D-latch. Here using CMOS-180nm technology. Ring oscillator using as a delay element, which is reduce the area. So we can achieve small amount of area than other delay element. That is buffer, D-latch. Buffer using as a delay element, which is reduce the delay of signal transmission. So we can improve the speed of the signal transmission than other delay element (ring oscillator, d-latch). D-latch using as a delay element, we can reduce the power consumption. The above table shows the simulation result.

B. CONCLUSION

Global interconnects form a major bottleneck for performance of digital system at scaled down technology. Use of current mode signalling is promising to remove this bottleneck. Through simulation we have demonstrated that current mode signalling bias scheme has overwhelming advantages over the current mode signalling feedback schemes. We have demonstrated that the particular configuration suggested by us for a current mode scheme is superior to other current mode schemes. Our scheme is robust with respect to batch to batch parametric variations and to on chip parametric variation. Therefore we assert that it is a practical option for use in modern systems for implementing both unidirectional and bidirectional data links.

This paper discusses about improvement in performance of signal transmission over long on-chip interconnects. To achieve this aim, the project was carried out with following objectives. CMS (Current Mode Signalling) with bias scheme which is used to provide low power consumption and high speed data transmission over long on-chip interconnect.

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