A Controlled Strategy of Three-Phase Four-Wire UPQC Topology With Reduced Dc-Link Voltage Rating

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Abstract—The unified power quality conditioner (UPQC) is a custom power device, which mitigates voltage and current-related PQ issues in the power distribution systems. In this paper, a UPQC topology using ANN controller for applications with non-stiff source is proposed. The proposed topology enables UPQC to have a reduced dc-link voltage without compromising its compensation capability. This proposed topology also helps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC. The topology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter. The average switching frequency of the switches in the VSI also reduces; consequently the switching losses in the inverters reduce. Detailed design aspects of the series capacitor and VSI parameters have been discussed in the paper. The present work deal with the control strategies based on ANN controller of the UPQC in detail for a 3phase three wire systems. The control strategies are modeled using MATLAB/SIMULINK. The performance is also observed under influence of utility side disturbances such as harmonics, flicker and spikes. The simulation results are listed in comparison of different control strategies and for the verification of results.

Index Terms—Average switching frequency, dc-link voltage, hybrid topology, non-stiff source, unified power quality conditioner (UPQC), ANN controller.

I. INTRODUCTION

Power Quality (PQ) has become an important issue since many loads at various distribution ends like adjustable speed drives, process industries, printers, domestic utilities, computers, microprocessor based equipments etc. have become intolerant to voltage fluctuations, harmonic content and interruptions.

Power Quality (PQ) mainly deals with issues like maintaining a fixed voltage at the Point of Common Coupling (PCC) for various distribution voltage levels irrespective of voltage fluctuations, maintaining near unity power factor power drawn from the supply, blocking of voltage and current unbalance from passing upwards from various distribution levels, reduction of voltage and current harmonics in the system and suppression of excessive supply neutral current.. Unified PQ conditioner (UPQC) is a versatile custom power device which consists of two inverters connected back-to-back and deals with both load current and supply voltage imperfections. UPQC can simultaneously act as shunt and series active power filters. The series part of the UPQC is known as dynamic voltage restorer (DVR). It is used to maintain balanced, distortion free nominal voltage at the load. The shunt part of the UPQC is known as distribution static compensator (DSTATCOM), and it is used to compensate load reactive power, harmonics and balance the load currents thereby making the source current balanced and distortion free with unity power factor. Voltage rating of dc-link capacitor largely influences the compensation performance of an active filter . In general, the dc-link voltage for the shunt active filter has much higher value than the peak value of the line-to-neutral voltage. This is done in order to ensure a proper compensation at the peak of the source voltage. In, the authors mentioned about the current distortion limit and loss of control limit, which states that the dc-link voltage should be greater than or equal to √6 times the phase voltage of the system for distortion free compensation. When the dc-link voltage is less than this limit, there is insufficient resultant voltage to drive the currents through the inductances so as to track the reference currents. The primary condition for reactive power compensation is that the magnitude of reference dc-bus capacitor voltage should be higher than the peak voltage at the point of common coupling (PCC). Due to the aforementioned criteria, many researchers have used a higher value of dc capacitor voltage based on applications. Similarly, for series active filter, the dc-link voltage is maintained at a value equal to the peak of the line-to-line voltage of the system for proper compensation . In case of the UPQC, the dc-link voltage requirement for the shunt and series active filters is not the same. Thus, it is a challenging task to have a common dc-link of appropriate rating in order to achieve satisfactory shunt and series compensation. The shunt active filter requires higher dc-link voltage when compared to the series active filter for proper compensation. In order to have a proper compensation for both series and shunt active filter, the researchers are left with no choice rather than to select common dc-link voltage based on shunt active filter requirement. This will result in over rating of the series active filter as it requires less dc-link voltage compared to shunt active filter. Due to this criterion, in literature, a higher dc link voltage based on the UPQC topology has been suggested. With the high value of dc-link capacitor, the voltage source inverters (VSIs) become bulky, and the switches used in the VSI also need to be rated for higher value of voltage and current. This in turn increases the entire cost and size of the VSI. To reduce the dc-link voltage storage capacity, few attempts were made in literature. In a hybrid filter has been discussed for motor drive applications. The filter is connected in parallel with diode rectifier and

tuned at seventh harmonic frequency. Although an elegant work, the design is specific to the motor drive application, and the reactive power compensation is not considered, which is an important aspect in UPQC applications. In case of the three-phase four-wire system, neutral-clamped topology is used for UPQC. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor voltage balancing. In four-leg VSI topology for shunt active filter has been proposed for three-phase four-wire system. This topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, in the authors proposed a T-connected transformer and three-phase VSC based DSTATCOM. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer. In this paper, a UPQC topology with reduced dc-link voltage is proposed. The topology consists of capacitor in series with the interfacing inductor of the shunt active filter. The series capacitor enables reduction in dc-link voltage requirement of the shunt active filter and simultaneously compensating the reactive power required by the load, so as to maintain unity power factor, without compromising its performance. This allows us to match the dc-link voltage requirements of the series and shunt active filters with a common dc-link capacitor. Further, in this topology, the system neutral is connected to the negative terminal of the dc bus. This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables independent control of each leg of the shunt VSI with single dc capacitor. The simulation studies are carried out using MATLAB, and detailed results are presented in the paper.

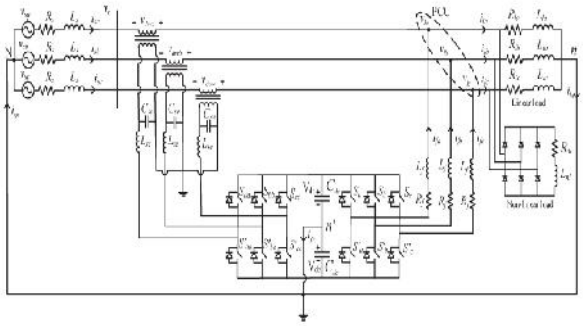


Fig. 1. Equivalent circuit of neutral-clamped VSI topology-based UPQC.

II. CONVENTIONAL AND PROPOSED TOPOLOGIESOF UPQC

In this section, the conventional and proposed topology of the UPQC are discussed in detail. Fig. 1 shows the power circuit of the neutral-clamped VSI topology-based UPQC which is considered as the conventional topology in this study. Even though this topology requires two dc storage devices, each leg of the VSI can be controlled independently, and tracking is smooth with less number of switches when compared to other VSI topologies. In this figure, *vsa*, *vsb*, and *vsc* are source voltages of phases *a*, *b*, and *c*, respectively. Similarly, *vta*, *vtb*, and *vtc* are terminal voltages. The voltages *v*dvr*a*, *v*dvr*b*, and *v*dvr*c* are injected by the series active filter. The three phase source currents are represented by *isa*, *isb*, and *isc*, load currents are represented by *ila*, *ilb*, and *ilc*. The shunt active filter currents are denoted by *ifa*, *ifb*, *ifc*, and *iln* represents the current in the neutral leg. *Ls* and *Rs* represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance of the shunt active filter are represented by *Lf* and *Rf* , respectively, and the interfacing inductance and filter capacitor of the series active filter are represented by *L*se and *C*se, respectively. The load constituted of both linear and nonlinear loads as shown in this figure. The dc-link capacitors and voltages across them are represented by *C*dc1 = *C*dc2 = *C*dc and *V*dc1 = *V*dc2 = *V*dc, respectively, and the total dc-link voltage is represented by *Vd*bus(*V*dc1 + *V*dc2 = 2*V*dc). In this conventional topology, the voltage across each common dc-link capacitor is chosen as 1.6 times the peak value of the source voltages as given in. Fig. 2 represents the equivalent circuit of the proposed VSI topology for UPQC comp nsated system. In this topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitor *Cf* in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology. The passive capacitor *Cf* has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the shunt active filter will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. This concept will be illustrated with analytic description in the following section. The reduction in the dc-link voltage requirement of the shunt active filter enables us to the match the dc-link voltage requirement with the series active filter. This topology avoids the over rating of the series active filter of the UPQC compensation system. The design of the series capacitor *Cf* and the other VSI parameters have significant effect on the performance of the compensator. These are given in the next section. This topology uses a single dc capacitor unlike the neutral-clamped topology and consequently avoids the need of balancing the dc-link voltages. Each leg of the inverter can be controlled independently in shunt active filter. Unlike the topologies mentioned in the literature this topology does not require the fourth leg in the shunt active filter for three-phase four-wire system. The performance of this topology will be explained in detailed in the following section.

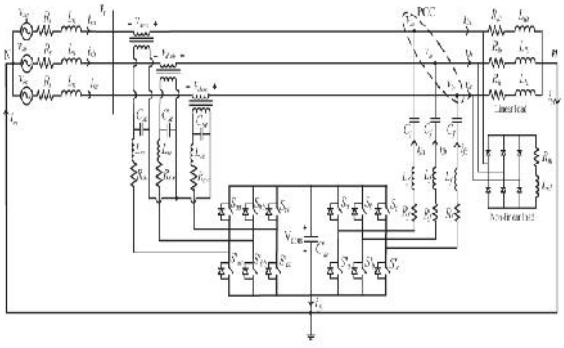


Fig. 2. Equivalent circuit of proposed VSI topology for UPQC compensated system.

III. DESIGN OF VSI PARAMETERS

The parameters of the VSI need to be designed carefully for better tracking performance. The important parameters that need to be taken into consideration while designing conventional VSI are *V*dc, *C*dc, *Lf* , *L*se, *C*se, and switching frequency (*f*sw). The design details of the VSI parameters for the shunt and series active filter are given in. Based on the following equations, the parameters of the VSIs are chosen for study.

A. Design of Shunt Active Filter VSI Parameters

Consider the active filter is connected to an X kVA system
and deals with 0.5X kVA and 2X kVA handling capability under transient conditions for *n* cycles. During transient, with an increase in system kVA load, the voltage across each dc-link capacitor (*V*dc) decreases and vice versa. Allowing a maximum of 25% variation in *V*dc during transient, the differential energy (Δ*Ec*) across *C*dc is given by

$$\Delta E_c = \frac{C_{\rm dc}\left[(1.125V_{\rm dc})^2 - (0.875V_{\rm dc})^2\right]}{2}. \qquad (1)$$

The change in system energy (Δ*Es*) for a load change from 2X kVA to 0.5X kVA is

$$\Delta E_s = (2X - X/2)nT. \qquad (2)$$

Equating (1) and (2), the dc-link capacitor value is given by

$$C_{\rm dc} = \frac{2(2X - X/2)nT}{(1.125V_{\rm dc})^2 - (0.875V_{\rm dc})^2}. \qquad (3)$$

where, *Vm* is the peak value of the source voltage, *X* is the kVA rating of the system, *n* is number of cycles, and *T* time period of each cycle.

An empirical study has been carried out for various values of interfacing inductance values with the variation of the dc-link voltage in with *V*dc = *Vm*, and it is found that *m* = 1.6 gives fairly good switching performance of the VSI. The approximate relationship between *m* and minimum (*f*swmin), maximum switching frequency (*f*swmax) is obtained by analysis of the VSI in and this is given below. For switching frequency variation approximately from 6 kHz to
10 kHz, the value of m is 1.58, which is taken as 1.6 in the study

$$m = \frac{1}{\sqrt{1 - f_{\rm swmin}/f_{\rm swmax}}}. \qquad (4)$$

Based on this, the shunt interfacing inductance has been derived taking into consideration of the maximum switching frequency and is given below

$$L_f = \frac{mV_m}{4h_1 f_{\rm swmax}} \qquad (5)$$

Where

$$h_1 = \sqrt{\frac{k_1}{k_2}\frac{(2m^2 - 1)}{4m^2} f_{\rm swmax}} \qquad (6)$$

where, *h*1 is the hysteresis band limit, *k*1 and *k*2 are proportionality constants.

B. Design of Series Active Filter VSI Parameters

In order to make the series active filter system a first-order system, a resistor is added in series with the filter capacitor, referred as switching band resistor (*R*sw).
The rms value of the capacitor current can be expressed as *I*se = _*I*2inv − *I*2*l* . *I*inv is the series inverter current rating and *Il* is the load current. The capacitor branch current is divided into two components—a fundamental current *I*se1, corresponding to the fundamental reference voltage (*V*ref1) and a switching frequency current *I*sw, corresponding to the band voltage (*V*sw).
The DVR voltage and the current of the capacitor are given by

$$V_{dvr} = \sqrt{V_{ref1}^2 + V_{\rm sw}^2}$$

$$I_{\rm se} = \sqrt{I_{\rm se1}^2 + I_{\rm sw}^2}$$

$$V_{\rm sw} = I_{\rm sw}R_{\rm sw} = \frac{h_2}{\sqrt{3}}$$

$$V_{\rm ref1} = I_{\rm se1}X_{\rm se1} = \frac{I_{\rm se1}}{2\pi f_1 C_{\rm se}} \qquad (7)$$

where *h*2 is the hysteresis band voltage.

The resistance (*R*sw) and the capacitance (*C*se) values are expressed in terms of band voltage *v*sw and rated references voltage (*V*ref1), respectively, and are given by

$$R_{\rm sw} = \frac{h_2}{I_{\rm sw}\sqrt{3}}$$

$$C_{\rm se} = \frac{I_{\rm se1}}{V_{\rm ref1}2\pi f_1}. \qquad (8)$$

The interfacing inductor *L*se has been designed based on the switching frequency of the series active filter and is given by

$$L_{\rm se} = \frac{(V_{\rm bus})R_{\rm sw}}{4f_{\rm swmax}h_2} \qquad (9)$$

where *Vbus* is the total dc-link voltage across both the dc-link capacitors.

A design example is illustrated for a rated voltage of 230 V line to neutral and the dc-link voltage reference (*V*dcref) of the conventional VSI topology has been taken as 1.6 *Vm* for each capacitor [27], [31]. The hysteresis band (*h*1) is taken as 0.5 A. From (5), the interfacing inductance (*Lf*) is computed to be 26 mH. The base kVA rating of the system is taken as 5 kVA. Using (3), *C*dc is computed and found to be 2200 μF. The rated series VSI voltage is chosen as 50% of the rated voltage, i.e., the maximum injection capacity of the series active filter is 115 V. The hysteresis band (*h*2) for series active filter is taken as 3% of the rated voltage, i.e., 6.9 V. The maximum switching frequency of the IGBT-based inverter is taken as 10 kHz. The series active filter current rating is choose as 8 A and the rated load current as 7 A. Using the the filter capacitor *C*se, the band resistor *R*sw and interfacing inductance *L*se are calculated to be 80 μF, 1.5 Ω, and 5 mH, respectively. The system parameters are given in Table I for the conventional VSI topology.

TABLE I
SYSTEM PARAMETERS

System Quantities	Values
System voltages	230 V (line to neutral), 50 Hz
Feeder impedance	$Z_s = 1 + j3.141\ \Omega$
Linear Load	$Z_{la} = 34 + j47.5\ \Omega$, $Z_{lb} = 81 + j39.6\ \Omega$, $Z_{lc} = 31.5 + j70.9\ \Omega$
Non-linear Load	three-phase full bridge rectifier load feeding a R-L load of 150 Ω-300 mH
Shunt VSI parameters	$C_{dc} = 2200\ \mu$F, $L_f = 26$ mH, $R_f = 1\ \Omega$ $V_{dbus} = 2 \times V_{dc} = 1040$ V (Conventional), $V_{dbus} = 560$ V(Proposed)
Series VSI parameters	C_{sc}=80 μF, L_{sc}= 5 mH $R_{sw} = 1.5\ \Omega$
Series interfacing transformer	1:1, 100 *V* and 700 *VA*
PI controller gains	$K_p = 6$, $K_i = 5.5$
Hysteresis band	$h_1 = \pm 0.5$ A, $h_2 = \pm 6.9$ V

C. Design of Cf for the Proposed VSI Topology

The design of the *Cf* depends upon the value to which the dc-link voltage is reduced. In general, loads with only nonlinear components of currents are very rare, and most of the electrical loads are combination of the linear inductive and nonlinear loads. Under these conditions, the proposed topology will work efficiently. The design of the value of *Cf* is carried out at the maximum load current, i.e., with the minimum load impedance to ensure that the designed *Cf* will perform satisfactorily at all other loading conditions. If *S*max is the maximum kVA rating of a system and *V*base is the base voltage of the system, then the minimum impedance in the system is given as

$$Z_{\min} = \frac{V_{\text{base}}^2}{S_{\max}} = |R_l + jX_l| \text{ (say)}. \tag{10}$$

In order to achieve the unity power factor, the shunt active filter current needs to supply the required reactive component of the load current, i.e., the fundamental imaginary part of the filter current should be equal to the imaginary part of the load current. The filter current and load current in a particular phase are given below

$$I_{\text{filter}} = \frac{V_{\text{inv1}} - V_{l1}}{R_f + j(X_{lf} - X_{cf})} \tag{11}$$

$$I_{\text{load}} = \frac{V_{l1}}{R_l + jX_l} \tag{12}$$

where, *Xlf* = 2*πfLf* , *Xl* = 2*πfLl*, *Xcf* = 1/2*πfCf* , and *f* is the supply frequency of fundamental voltage.
Neglecting the interfacing resistance and equating the imaginary parts of the the above equations gives

$$\frac{V_{l1}X_l}{R_l^2 + X_l^2} = \frac{V_{\text{inv1}} - V_{l1}}{(X_{lf} - X_{cf})^2}(X_{lf} - X_{cf}) \tag{13}$$

where, *V*inv1 and *Vl*1 are the line to neutral rms voltage of the inverter and the PCC voltage at the fundamental frequency, respectively. The fundamental component of inverter voltage in terms of dc-link voltage is described in as given below

$$V_{\text{inv1}} = \frac{0.612V_{\text{dc}}}{2\sqrt{3}}. \tag{14}$$

In general, if the filter current (*If*) flows from the inverter terminal to the PCC, the voltage at the inverter terminal should be at a higher potential. Due to this reason, in conventional VSI topologies, the dc-link voltage is maintained higher than the voltage at the PCC. Equations (15) and (16) give the KVL along the filter branch for conventional topology and the proposed modified topology, respectively

$$uV_{\text{dc}} - v_l = L_f\frac{di_f}{dt} + R_f i_f \tag{15}$$

$$\left(uV_{\text{dc}} - \frac{1}{C_f}\int i_f dt\right) - v_l = L_f\frac{di_f}{dt} + R_f i_f$$

$$(uV_{\text{dc}} - v_{cf}) - v_l = L_f\frac{di_f}{dt} + R_f i_f \tag{16}$$

where, *u* attains values of 1 or −1 depending on the switching of the inverter.

In the fundamental voltage across the capacitor (*vcf*1) adds to the inverter terminal voltage (*uV*dc) when the load is inductive in nature. This is because, when the load is inductive in nature, the fundamental of the filter current leads the voltage at the PCC by 90◦ for reactive power compensation, and thus the fundamental voltage across the capacitor again lags the fundamental filter current by 90◦. Therefore, the fundamental voltage across the capacitor will be in phase opposition to the voltage at the PCC. Thus, the fundamental voltage across the capacitor adds to the inverter terminal voltage. This allows us to rate the dc-link voltage at lower value than conventional design. The designer has a choice to choose the value of dc-link voltage to be reduced,

such that the LC filter in the active filter leg of each phase offers minimum impedance to the fundamental frequency and higher impedance for switching
frequency components.

In the modified topology along with the series capacitor in the shunt active filter, the system neutral is connected to the negative terminal of the dc bus capacitor. This will introduce a positive dc voltage component in the inverter output voltage. This is because, when the top switch is "ON," +*Vd*bus appears at the inverter output, and 0 V appears when the bottom switch is "ON." Thus, the inverter output voltage will have dc voltage component along with the ac voltage. The dc voltage is blocked by the series capacitor, and thus the voltage across the series capacitor will be having two components, one is the ac component, which will be in phase opposition to the PCC voltage, and the other is the dc component. Whereas, in case of the conventional topology, the inverter output voltage varies between +*V*dc when top switch is "ON" and −*V*dc when the bottom switch "ON." Similarly, when a four-leg topology is used for shunt active filter with a single dc capacitor, the inverter output voltage varies between +*Vd*bus and −*Vd*bus. Therefore, these topologies does not contain any dc component in the inverter output voltage.

The modified topology contains only one dc capacitor as the neutral is directly connected to the negative terminal of the dc bus, thus it avoids the need of balancing of capacitor voltages, which is a major disadvantage of the neutral-clamped topology. Since the neutral wire is directly connected to the negative terminal of the dc bus, the necessity of fourth leg in the inverter is avoided. In case of the four-leg-based VSI topology, independent control is not possible. In the modified topology, the three legs of the shunt active filter are independently controlled, and this results in the automatic tracking of the neutral current. Thus, the modified topology has the advantage of both
the neutral-clamped topology and four-leg inverter topology.

From the system parameters mentioned in Table I, phase-*a* load impedance is chosen as *Z*min. The dc bus voltage is chosen to be 560 V for the modified topology, such that it matches with the dc-link voltage requirement of the series active filter (peak of the line to line voltage). Using (13), the value of the the capacitor (*Cf*) is obtained to be 65 μF.

IV. GENERATION OF REFERENCE COMPENSATOR CURRENTS UNDER UNBALANCED AND DISTORTED VOLTAGES

In this work, the load currents are unbalanced and distorted, these currents flow through the feeder impedance and make the voltage at terminal unbalanced and distorted. The series active filter makes the voltages at PCC balanced and sinusoidal. However, the voltages still contain switching frequency components and they contain some distortions. If these terminal voltages are used for generating the shunt filter current references, the shunt algorithm results in erroneous compensation. To remove this limitation of the algorithm, fundamental positive sequence voltages $v^+_{la}1(t)$, $v^+_{lb}1(t)$, and $v^+_{lc}1(t)$ of the PCC voltages are extracted and are used in control algorithm for shunt active filter. The expressions for reference compensator currents are given in (17). In this equation, *Pl*avg is the average load power, *P*loss denotes the switching losses and ohmic losses in actual compensator, and it is generated using a capacitor voltage ANN controller. The term *Pl*avg is obtained using a moving average filter of one cycle window of time *T* in seconds. The term ϕ is the desired phase angle between the source voltage and current

$$i^*_{fa}=i_{la}-i^*_{sa}=i_{la}-\frac{v^+_{la1}+\gamma\left(v^+_{lb1}-v^+_{lc1}\right)}{\Delta^+_1}(P_{\text{lavg}}+P_{\text{loss}})$$

$$i^*_{fb}=i_{lb}-i^*_{sb}=i_{lb}-\frac{v^+_{lb1}+\gamma\left(v^+_{lc1}-v^+_{la1}\right)}{\Delta^+_1}(P_{\text{lavg}}+P_{\text{loss}})$$

$$i^*_{fc}=i_{lc}-i^*_{sc}=i_{lc}-\frac{v^+_{lc1}+\gamma\left(v^+_{la1}-v^+_{lb1}\right)}{\Delta^+_1}(P_{\text{lavg}}+P_{\text{loss}}) \quad (17)$$

Where

$$\Delta=\sum_{j=a,b,c}\left(v^+_{lj1}\right)^2,\gamma=\tan\varphi/\sqrt{3}.$$

The above algorithm gives balanced source currents after compensation irrespective of unbalanced and distorted supply.

The reference voltages for series active filter are given as

$$v^*_{\text{dvr}i}=v^*_{li}-v_{ti}$$
$$i=a,b,c \qquad (18)$$

where $v*li$ represents the desired load voltages in three phases, and $v*$dv*ri* represents the reference series active filter voltages.

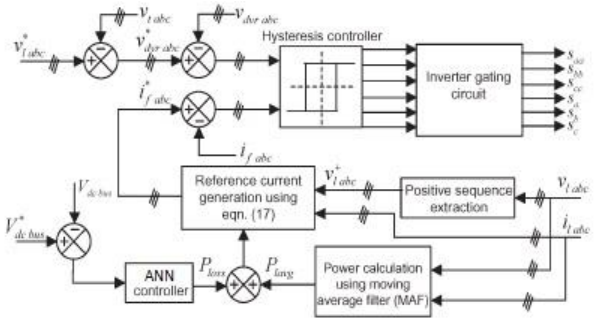


Fig. 3. Control block diagram for UPQC.

Once the reference quantities and the actual quantities are obtained from the measurements, the switching commands for the VSI switches are generated using hysteresis band current control method. Hysteresis current controller scheme is based on a feedback loop, generally with two-level comparators. The switching commands are issued whenever the error limit exceeds a specified tolerance band "±*h*." Unlike the predictive controllers, the hysteresis controller has the advantage of peak current limiting capacity apart from other merits such as extremely good dynamic performance, simplicity in implementation and independence from load parameter variations. The disadvantage with this hysteresis method is that the converter switching frequency is highly dependent on the ac voltage and varies with it.

V. SIMULATION RESULTS

In order to validate the proposed topology, simulation is carried out using MATLAB. The same system parameters which are given Table I with additional *Cf* for a desired dc-link voltage are used to carry out simulation studies. The simulation results for both the conventional topology and the proposed modified topology are presented in this section for better understanding and comparison between both the topologies. simulation figure shown below,

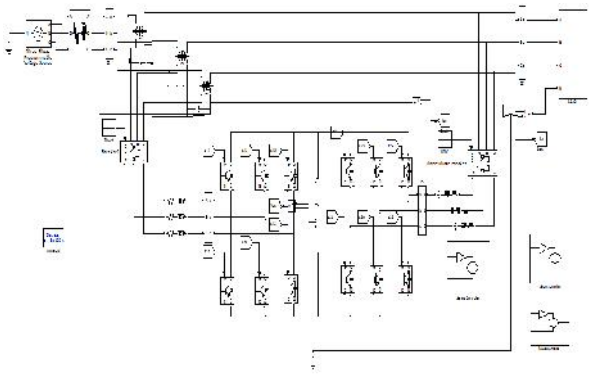


Fig 1 a Model Three-Phase Four Wire UPQC Topology with Reduced DC-Link Voltage Rating Using ANN

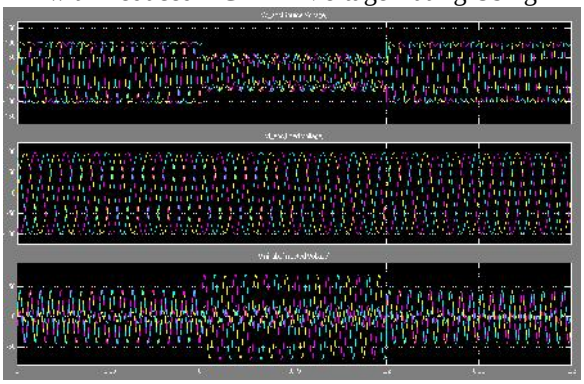
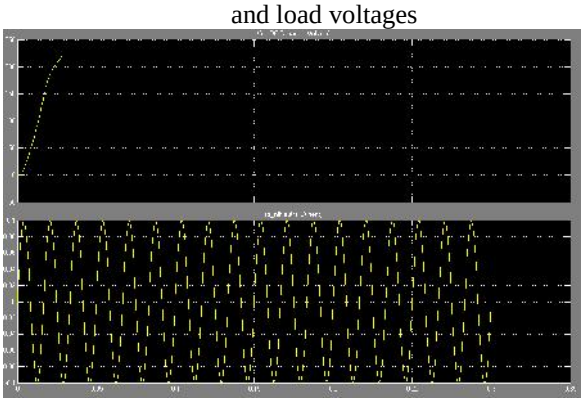


Fig 2 Terminal Voltages With Sag, DVR injected voltages, and load voltages



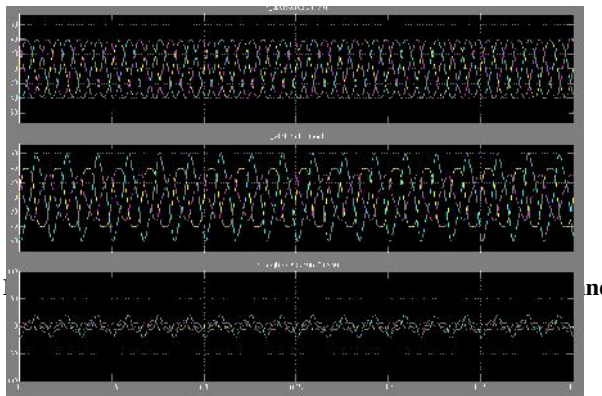


Fig 3 DC capacitor voltages and injected current.

Fig 4 Source current and load current, injected shunt current.

The load currents and terminal (PCC) voltages before compensation are shown in Fig. 2. The load currents are unbalanced and distorted as shown in Fig. 3, the terminal voltages are also unbalanced and distorted because these load currents flow through the feeder impedance in the system as shown in Fig. 4. gives the simulation results of the UPQC using conventional VSI topology. The dc-link voltages across the top and bottom dc-link capacitors are shown in Fig. 3. Using PI controller, the voltage across both dc capacitors are maintained constant to a reference value of 520 V as shown in he figure. The source currents after compensation are balanced and sinusoidal.The voltage across the interfacing inductor in phase-*a* is shown in Fig. 4. The peak to peak voltage across the inductor is 1040 V. The three-phase shunt compensator currents are shown in Fig. . Fig. 5(e) represents the compensation performance of the series active filter. A sag of 50% is considered in all phases of the the terminal voltages for five cycles, which start from 1.9 s and ends at 2.0 s. The compensated DVR voltages and load voltages after compensation are shown in the same figure. The load voltages are maintained to the desired voltage using series active filter.

VI. CONCLUSION

A modified UPQC topology for three-phase four-wire system using ANN controller has been proposed in this paper, which has the capability to compensate the load at a lower dc-link voltage under non stiff source. Design of the filter parameters for the series and shunt active filters is explained in detail. The proposed method is validated through simulation and experimental studies in a three-phase distribution system with neutral-clamped UPQC topology (conventional). The proposed modified topology gives the advantages of both the conventional neutral-clamped topology and the four-leg topology.

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