Power Quality Enhancement of Three Level Inverter using SVPWM Fed Induction Motor Drive

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Abstract— The modelling and simulation of modified SVPWM VSI fed three phase Induction motor drive are also presented. The drive system is modelled using the blocks of simulink The Z-source inverter is a relatively recent converter topology that exhibits both voltage-buck and voltage-boost capa-bility. The Z-source concept can be applied to all dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion whether two-level or multilevel. Power electronic inverter is a circuit that converts direct power to
alternative power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. It is widely used in industrial power conversion systems both for utility and drives applications. Induction motor is popularly used in industries due to ruggedness and robustness. Previous publications have shown the control of a Z-source neutral point clamped inverter using the carrier-based modulation technique. Z-source inverter based adjustable speed drive system (ASD) effectively uses the shoot-through state to boost DC bus voltage by simultaneously gating on both the upper and lower switches of a same phase leg. The shoot-through zero state has no harmful effect on the inverter and is used to boost the DC link voltage. This paper presents the control of a Z-source neutral point clamped inverter using the space vector modulation technique. This gives a number of bene-fits, both in terms of implementation and harmonic performance. The adopted approach enables the operation of the Z-source ar-rangement to be optimized and implemented digitally without in-troducing any extra commutations. The proposed techniques are demonstrated both in simulation and through experimental results from a prototype converter.

Index Terms—Buck–boost, neutral point clamped inverter, space vector modulation (SVM),Induction Motor,Z-source inverter.

I. INTRODUCTION

MANY industrial applications require higher power con-verters (inverters) which are now almost exclusively im-plemented using one of the multilevel types. Multilevel con-verters offer many benefits for higher power applications which include an ability to synthesize voltage waveforms with lower harmonic content than two-level converters and operation at higher dc voltages using series connection of a basic switching cell of one type or another [1]–[4].

Even though many different multilevel topologies have been proposed, the three most common topologies are the cascaded inverter [5]–[7], the diode clamped inverter [8]–[12], and the ca-pacitor clamped inverter [13]–[15]. Among the three, the three-level diode clamped [also known as the neutral point clamped (NPC)] inverter has become an established topology in medium voltage drives and is arguably the most popular [16]–[19]— certainly for three-level circuits. However, the NPC inverter is constrained by its inability to produce an output line-to-line voltage greater than the dc source voltage. For applications where the dc source is not always constant, such as a fuel cell [20], [21], photovoltaic array [22], and during voltage sags, etc., a dc/dc boost converter is often needed to boost the dc voltage to meet the required output voltage or to allow the nominal operating point to be favorably located [23], [24]. This increases the system complexity and is desirable to eliminate if possible.

The main function of a multilevel inverter is to produce a desired AC voltage level from several DC voltage sources. This DC voltage source may or may not be equal to one another. The AC voltage produced from this DC voltage appears to be a sinusoidal. One pitfall of using multilevel inverter is to approximate sinusoidal waveforms concern with harmonics. The staircase waveform produced by a multilevel inverter contains sharp transitions. The harmonics which are generated, in addition to the fundamental frequency of the sinusoidal waveform are analyzed using the Fourier Series Theory. The harmonics generated on the AC side greatly influence the power quality of the control system. The multilevel inverter improves the AC power quality by performing the power conversion in small voltage steps leading to lower harmonics. For this reason, researchers are doing considerable work on multilevel inverter in recent years.

The Z-source inverter [25] topology was proposed to over-come the above limitations in traditional inverters. The Z-source concept can be applied to all dc-to-ac [26], ac-to-dc [27], ac-to-ac [28]–[31], and dc-to-dc [32], [33] power conversion whether two-level or multilevel. The Z-source concept was extended to the NPC inverter in [34], where two additional Z-source net-works were connected between two isolated dc sources and a traditional NPC inverter. In spite of its effectiveness in achiev-ing voltage buck–boost conversion, the Z-source NPC inverter proposed in [34] is expensive because it uses two Z-source networks, two isolated dc sources, and requires a complex mod-ulator for balancing the boosting of each Z-source network. To overcome the cost and modulator complexity issues, the design and control of an NPC inverter using a single Z-source network was presented in [35]. The operational analysis and optimal con-trol of the reduced element count (REC) Z-source NPC inverter was subsequently described in [36].

The REC Z-source NPC inverter is expected to find appli-cations in grid connected distributed generation (DG) systems based on renewable energy sources such as photovoltaic sys-tems, wind turbines, and fuel cell stacks [37]. Two DG systems can be connected to the grid with only one REC Z-source NPC inverter, thus reducing the volume and cost while increasing efficiency and facilitating control. The power quality of current injected to the grid is improved because of the three-level struc-ture. It can also find use in adjustable speed drive systems in applications such as conveyor belts, fans, and water pumps [38].

In [36], the modulation of the REC Z-source NPC inverter was described using the carrier-based approach. However, the space vector modulation (SVM) approach offers better

harmonic per-formance [11] (compared with carrier-based pulsewidth modu-lation (PWM) strategy without zero-sequence voltage injection) and can more conveniently handle overall switching patterns and constraints [39], [40], and it is simple to implement us-ing a DSP [41]. The contribution of this paper is, therefore, the development of a modified SVM algorithm for controlling the REC Z-source NPC inverter. The theoretical development is discussed in detail, and simulations as well as experimental re-sults are used to verify the operation of the circuit and proposed SVM-based modulation.

Application of ASDs in commercial and industrial sectors is increasing due to their improved efficiency, energy savings, and effective control. There are two traditional power inverter topologies surviving for induction motor drive applications: voltage source inverter (VSI) and current source inverter (CSI). In these inverters, a DC voltage/current source supported by a relatively large capacitor/inductor feeds the main three phase bridge inverter circuit. The DC voltage source could be a battery or output of a front end rectifier circuit connected with the utility AC supply or a capacitor. Six switches are used in the main circuit; each is traditionally composed of a power insulated gate bipolar junction transistor (IGBT) and an antiparallel (or feedback) diode to provide bidirectional current flow and unidirectional voltage blocking capability. Z-source inverter (ZSI) is a direct current (DC) to alternating current (AC) power conversion concept that is very promising in the areas of power conditioning especially in alternative energy sources, adjustable speed drives (ASD) and distributed generation.

II. REVIEW OF Z-SOURCE CONCEPT

The topology of a two-level Z-source inverter is shown in Fig. 1. The only difference between the Z-source inverter and a traditional voltage source inverter (VSI) is the presence of a Z-source network comprising a split-inductor (L_1 and L_2) and two capacitors (C_1 and C_2). The unique feature of the two-level Z-source inverter is that the output ac voltage fundamental can be controlled to be any value between zero and (theoretically) infinity regardless of the dc source voltage. Thus, the Z-source inverter is a buck–boost inverter that has a very wide range of obtainable output voltage. Traditional VSIs cannot provide such features.

In Fig. 1, the two-level Z-source inverter bridge has 15 permissible switching states unlike the traditional two-level VSI that has 8. The traditional three-phase VSI has six active states when the dc voltage is impressed across the load and two zero states when the load terminals are shorted through either the lower or upper three devices, respectively. However, the two-level Z-source inverter bridge has seven extra zero states (termed shoot-through states) when the load terminals are shorted through both upper and lower devices of any one phase leg (i.e., both devices are gated ON), any two phase legs, or all three phase legs. These shoot-through states are forbidden in a traditional VSI for obvious reasons. The Z-source network makes the shoot-through zero states possible and provides the means by which boosting operation can be obtained. Critically, any of the shoot-through states can be substituted for normal zero states without affecting the PWM pattern seen by the load.

Therefore, for a fixed switching cycle, insertion of shoot-through states within the zero intervals with the active state intervals maintained constant will not alter the normalized volt–second average per switching cycle seen by the ac load. Instead, with the shoot-through states inserted, the effective inverter dc link voltage V_i can be stepped up as given in (1) [25], [42]. Consequently, taking also the PWM modulation index M into account, the phase ac output voltage V_x (x∈_{a, b, c}) can be expressed by (2)

$$V_i = \frac{E}{\left(1-2.\frac{T_{ST}}{T}\right)} = B.E, B \geq 1 \qquad (1)$$

$$V_x = \frac{M.V_i}{\sqrt{3}} = B\left[ME/\sqrt{3}\right] \qquad (2)$$

where T_{ST} and T are the shoot-through interval and switching period, respectively, B is the boost factor and the term in parenthesis represents the phase ac output voltage of a traditional VSI. Equations (1) and (2) show that the ac output voltage of a Z-source inverter can be regulated from zero to the nor-mal maximum by altering M and maintaining B = 1, or can be boosted above that obtainable with a traditional VSI by choosing B > 1. A similar analysis can be carried out for the current-type Z-source inverter [43]. However, since the focus of this paper is that of the voltage-type Z-source inverter, the analysis for the current-type Z-source inverter would not be discussed further due to space limitation.

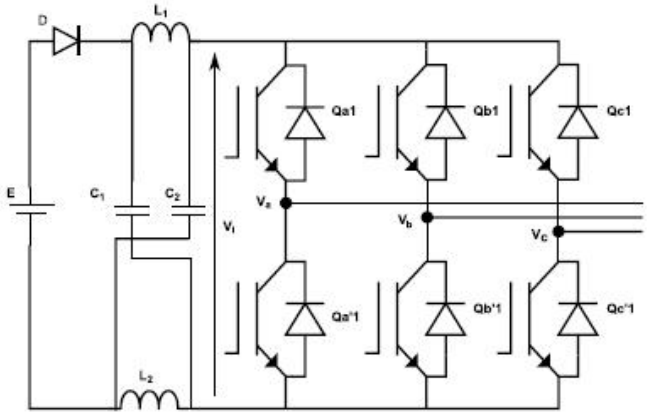


Fig. 1. Topology of two-level Z-source inverter.

III. TOPOLOGY OF REC Z-SOURCE NPC INVERTER

A. Extension of The Z-Source Concept to the NPC Inverter

To describe the operating principle of the REC Z-source NPC inverter shown in Fig. 2, we concentrate initially on the operation of one phase leg. The operation of each inverter phase leg of a traditional NPC inverter can be represented by three switching states P, O, and N. Switching state "P" denotes that the upper two switches in a phase leg are gated ON, "N" indicates that the lower two switches conduct, and "O" signifies that the inner two switches are gated ON.

However, each phase leg of the Z-source NPC inverter has three extra switching states which resemble the "O" state of the traditional NPC inverter. These extra switching states oc-cur when all the four switches in any phase leg are gated ON [full-shoot-through (FST)], or the three upper switches in any phase leg are gated ON [upper-shoot-through (UST)] or the three bottom switches in any phase leg are gated ON [lower-shoot-through (LST)]. These shoot-through states are forbidden in the

traditional NPC inverter because they would cause a short circuit of the dc-side capacitors. Again, the Z-source network makes these shoot-through states permissible and provides the means for boost operation.

TABLE I
SWITCHING STATES OF AN REC Z-SOURCE NPC INVERTER

State Type	ON Switches	ON Diodes	Vxo	Switching State
NST	Qx1,Qx2	D1,D2	$+V_i/2$	P
NST	Qx2,Qx'1	D1,D2,{Dx1 or Dx2}	0	O
NST	Qx'1,Qx'2	D1,D2	$-V_i/2$	N
FST	Qx1,Qx2,Qx'1, Qx'2	—	0	FST
UST	Qx1,Qx2,Qx'1	Dx2,D1	0	UST
LST	Qx2,Qx'1,Qx'2	Dx1,D2	0	LST

B. Circuit Analysis

Among the three-level Z-source power converter topologies reported to date, the Z-source NPC inverter implemented using a single LC impedance network (see Fig. 2) is considered to be an optimized topology in terms of component count [44], [45].

Referring to Fig. 2, the REC Z-source NPC inverter is supplied with a split dc source. The middle point O is taken as a reference. By controlling the switches of each phase leg according to the combinations presented in Table I, each output phase voltage V_{xo} (x_{a, b, c}) has three possibilities: V_i /2, 0, and $-V_i$ /2.

When the REC Z-source NPC inverter is operated without

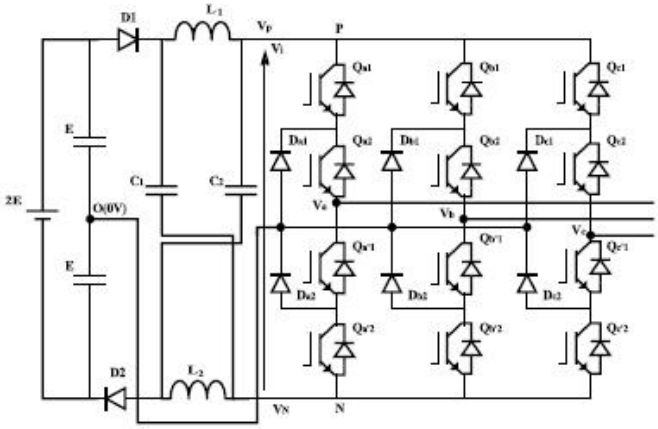


Fig. 2. Topology of an REC Z-source NPC inverter.

any shoot-through states, then V_i is equivalent to 2E. As noted earlier, with this kind of operation, the maximum obtainable output line-to-line voltage cannot exceed the available dc source voltage (2E). Therefore, to obtain an output line-to-line voltage greater than 2E, shoot-through states are carefully inserted into selected phase legs to boost the input voltage to V_i > 2E before it is inverted by the NPC circuitry. Thus, the REC Z-source inverter can boost and buck the output line-to-line voltage with a single-stage structure.

In [36], two new switching states namely the UST and LST states were identified, in addition to the FST state and the non-shoot-through (NST) states (P, O, and N) that had been reported earlier in [35]. Although operation using the FST and NST states is possible (termed the FST operating mode), it is generally preferable to use the UST and LST states in place of the FST states (termed the ULST operating mode). The ULST operating mode is preferred because it produces an output voltage with enhanced waveform quality.

The simplest FST operating mode requires all four switches in a phase leg (see Table I) to be turned ON. This is not a minimal loss approach since, for example, switching phase A from +E through FST to 0 V would require switches {Qa1, Qa2, Qa'1, Qa'2} changing from {ON, ON, OFF, OFF} through {ON, ON, ON, ON} to {OFF, ON, ON, OFF}. An alternative FST operating mode which gives minimal loss uses two phase legs to create the shoot-through path. This requires, for example, synchronization of the turn ON instants of switches Qa1 from phase A and Qc'2 from phase C at the start of an FST state. Doing so creates a time interval during which switches {Qa1, Qa2, Qa'1} from phase A and {Qc2, Qc'1, Qc'2} from phase C are gated ON simultaneously to create a shoot-through path [35].

However, the output line-to-line voltage obtained using the minimal loss FST approach has higher harmonic distortion (compared to the ULST approach) in its output voltage wave-form because the voltage levels produced do not have adjacent level switching [35]. Therefore, in this paper, the ULST op erating mode is used for controlling the REC Z-source NPC inverter. Fig. 3(a) shows the simplified equivalent circuit for the NST state, while Fig. 3(b) and (c) shows the UST and LST states. Note that there are multiple ways of creating the UST and LST states using different phases. The choice between these is discussed later. Assuming that the Z-source network is symmet-
rical ($L_1 = L_2 = L$ and $C_1 = C_2 = C$), then $V_{L\,1} = V_{L\,2} = V_L$ and $V_{C\,1} = V_{C\,2} = V_C$ and the voltage expressions for the NST state are as follows:

NST

$$V_L = 2E - V_C \tag{3}$$

$$V_P = +\frac{V_i}{2}, \quad V_N = -\frac{V_i}{2} \tag{4}$$

$$V_i = 2(V_C - E). \tag{5}$$

Similarly, the voltage expressions for the UST and LST states are as follows:

UST

$$V_{L_1} = E \tag{6}$$

$$V_P = 0\ \text{V}, \quad V_N = E - V_{C_1}. \tag{7}$$

LST

$$V_{L_2} = E \tag{8}$$

$$V_P = -E + V_{C_2}, \quad V_N = 0\ \text{V}. \tag{9}$$

We denote the duration of the NST, UST, and LST states by T_N , T_U , and T_L , respectively, and the switching period by T . Also, we assume that T_U and T_L are equal (this is necessary to ensure symmetrical operation) and denote the total combined UST and LST duration by $T_{U\,LST}$. At steady state, the average voltage across the inductors is zero; therefore, averaging the

inductor voltage over one switching period, we have

$$\frac{(2E - V_C) \cdot T_N + E \cdot T_U + E \cdot T_L}{T} = 0 \qquad (10)$$

$$T_N + T_U + T_L = T. \qquad (11)$$

Solving for V_C using (10) and (11), we have

$$V_C = (2E) \cdot \left\{ \frac{1 - T_{\mathrm{ULST}}/2T}{1 - T_{\mathrm{ULST}}/T} \right\}. \qquad (12)$$

Substituting (12) into (5), we have the dc-link voltage V_i during the NST state as

$$V_{i\_\mathrm{NST}} = \left\{ \frac{2E}{1 - T_{\mathrm{ULST}}/T} \right\}. \qquad (13)$$

Similarly, when (12) is substituted into (7) and (9) and noting that $V_i = V_P - V_N$, we have the dc-link voltage during the UST and LST states as

$$V_{i\_\mathrm{UST}} = V_{i\_\mathrm{LST}} = \left\{ E \left| \left(1 - \frac{T_{\mathrm{ULST}}}{T}\right) \right. \right\} \qquad (14)$$

It is noted from (13) and (14) that the higher dc-link voltage is present during the NST states and it is twice the dc-link voltage available during the UST and LST states, as required. The fundamental peak ac output voltage V_{xo} (x_{a, b, c}) is given by

$$\hat{V}_{xo} = \frac{M}{\sqrt{3}} \cdot V_{i\_\mathrm{NST}} \qquad (15)$$

$$\hat{V}_{xo} = \left(\frac{1}{1 - T_{\mathrm{ULST}}/T} \right) \left\{ \frac{M}{\sqrt{3}} (2E) \right\} = B' \left\{ \frac{M}{\sqrt{3}} (2E) \right\} \qquad (16)$$

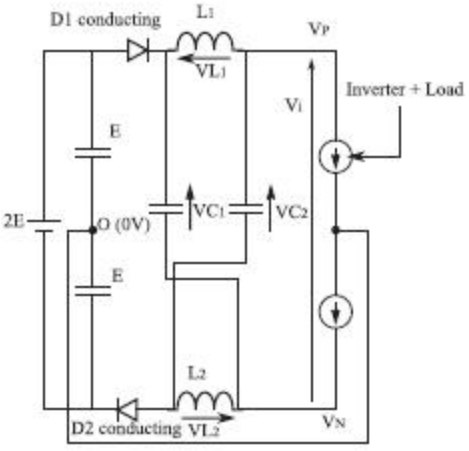


Fig. a

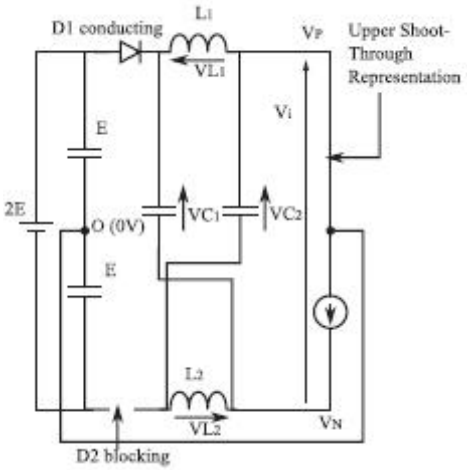


Fig. b

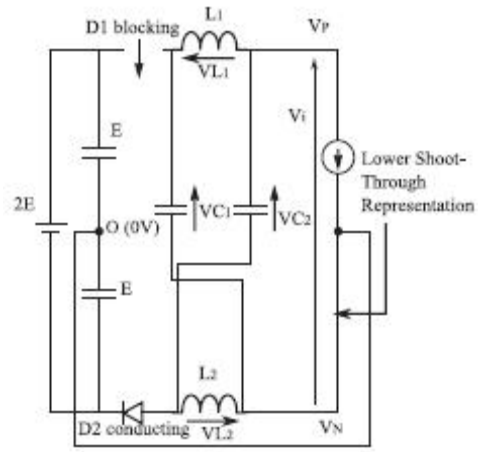


Fig. c

Fig. 3. Simplified representation of REC Z-source NPC inverter in (a) NST, (b) UST, and (c) LST states

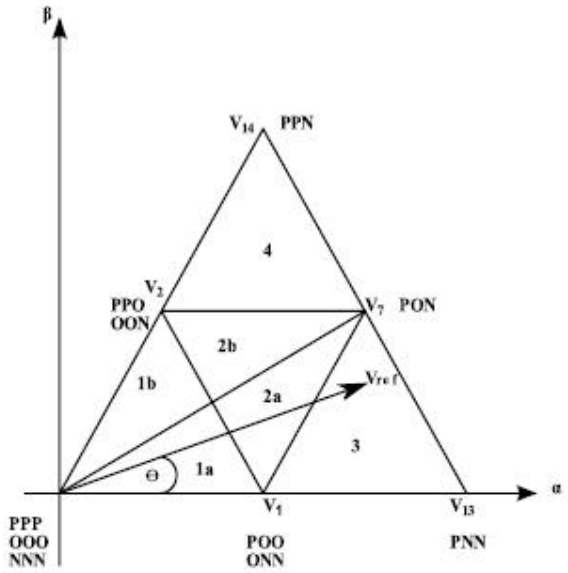


Fig. 4. Space vector diagram of sector 1 for a three-level inverter.

where $B^- \geq 1$ is the boost factor [44] and all the other symbols

IV. MODIFIED SVM OF THE REC Z-SOURCE NPC INVERTER

A. Duty Cycle Calculation

The space vector diagram of a raditional NPC inverter for sector 1 is shown in Fig. 4. The reference vector $\vec{V}_{ref}$ can be expressed as

$$V_{ref}(t) = \frac{2}{3}[V_{ra}(t)e^{j0} + V_{rb}(t)e^{j2\pi/3} + V_{rn}(t)e^{j4\pi/3}]. \quad (17)$$

Generally, in SVM, the reference vector $\vec{V}_{ref}$ is synthesized with three nearest space vectors, which are selected based on the triangle in which the reference vector is located at the sampling instant. If the reference vector is located in triangle 3, the nearest three vectors are $\vec{V}_1$, $\vec{V}_7$, and $\vec{V}_{13}$, respectively. Let the duty ratios of these vectors be denoted by d_1 , d_2 , and d3 , respectively. The modulation law with a sequence of the nearest three vectors based on the volt–second product is then as follows:

$$d_1 \cdot \vec{V}_1 + d_2 \cdot \vec{V}_7 + d_3 \cdot \vec{V}_{13} = \vec{V}_{\text{ref}}$$
$$d_1 + d_2 + d_3 = 1. \quad (18)$$

The voltage vectors $\vec{V}_1$, $\vec{V}_7$, $\vec{V}_{13}$, and $\vec{V}_{ref}$ in Fig. 4 can be expressed as

$$\vec{V}_1 = \frac{1}{3} \cdot (2E)$$
$$\vec{V}_7 = \frac{\sqrt{3}}{3} \cdot e^{j\pi/6} \cdot (2E)$$
$$\vec{V}_{13} = \frac{2}{3} \cdot (2E)$$
$$\vec{V}_{\text{ref}} = V_{\text{ref}} \cdot e^{j\theta}. \quad (19)$$

Substituting (19) into (18), the duty ratios of the nearest three voltage vectors are given by (20), where M is the modulation index and $0 \le \theta \le \pi/3$

$$d_1 = 2 - 2M \sin(\pi/3 + \theta)$$
$$d_2 = 2M \sin\theta$$
$$d_3 = 2M \sin(\pi/3 - \theta) - 1. \quad (20)$$

A similar procedure is used for calculating the duty ratios of the selected voltage vectors in all the other triangles. To complete the modulation process, the selected voltage vectors are applied to the output according to a switching sequence. Ideally, a switching sequence is formed in such away that a highquality output waveform is obtained with minimum number of switching transitions [46].

A. Switching Sequence and Insertion of Shoot-Through States

To achieve the minimal number of switches changing between two adjacent states, a seven-segment switching sequence is adopted in SVM. If the reference vector stays in triangle 3 (see Fig. 4), and using the decomposition method, where the null state is shifted from {PPP/OOO/NNN} to {POO/ONN}, the Equivalent Null (E-Null) states are V_1{POO} and V_1{ONN}, while the Equivalent Active (E-Active) states are V_7{PON} and V_{13}{PNN}, respectively. The seven-segment switching sequence in triangle 3 can then be briefly illustrated as shown in Table II [46]. In a traditional three-level NPC inverter, only switching transitions between the "P" state and the "O" state or the "N" state and the "O" state are permitted. Switching directly between the "P" state and the "N" state is not allowed because it results in all four switches changing state, which results in nonequal dynamic voltage and double the switching loss.

TABLE II
SEVEN-SEGMENT SWITCHING SEQUENCE IN TRIANGLE 3

	E-Null1	E-Active1	E-Active2	E-Null2	E-Active2	E-Active1	E-Null1
Segment	1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}	6^{th}	7^{th}
Vector	V_1	V_{13}	V_7	V_1	V_7	V_{13}	V_1
State	ONN	PNN	PON	POO	PON	PNN	ONN

TABLE III
PERMISSIBLE UST AND LST STATES

UST states	LST states
UNN	PLO
UON	POL
OUN	PPL
NUN	LPO
NUO	OPL
NOU	LPP
NNU	LOP
UNO	OLP
ONU	PLP

In order to introduce shoot-through states, it is necessary to determine where the UST and LST states can be inserted, and on which phase, in order that the normalized volt–second area applied to the load is unchanged from the standard NPC case discussed above. In addition, it is desirable to ensure that no extra commutations are introduced. Theoretically, a shoot-through state can be introduced on any phase which is switched to the zero level (O) without affecting that phase voltage. However, the effect on the line-to-line voltages must also be taken into account. Note that when any phase has UST applied, the positive rail (P) is at the same potential as the dc mid-point (O). Similarly, during LST, the negative rail (N) is at the same potential as the dc mid-point (O). Consequently, it is only possible to use the UST state on a given phase when it is connected to O and the other two phases are connected either to O or N in order to get the correct line-to-line voltages. Similarly, an LST state can only be used when the other two phases are O or P. Therefore, the permissible shoot-through states are as shown in Table III where "U" and "L" represent UST and LST states in a phase leg, respectively.

Taking the above into account, the objective is to deploy the UST/LST states for voltage boosting in an optimalway that does not increase the number of commutations. A modified PWM sequence which achieves this can be derived as discussed below. Fig. 5(a) shows the seven-segment PWM switching sequences for modulating a traditional NPC inverter and an REC Z-source NPC inverter when the reference vector, $\vec{V}_{ref}$ is in triangle 3 of the vector diagram shown in Fig. 4.

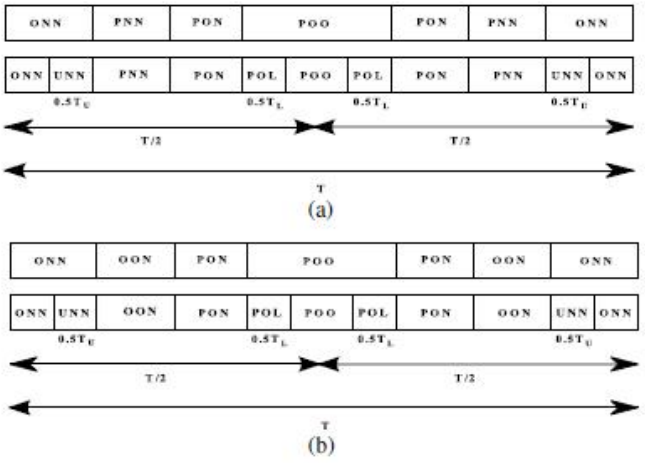


Fig. 5. Modulation of traditional NPC and Z-source NPC when the reference vector is in (a) triangle 3 and (b) triangle 2a on the three-level vector diagram shown in Fig. 4.

Comparing the sequences shown in Fig. 5(a), it is observed that the only difference between them is the insertion of a UST state in phase A to the left of the E-active state {PNN} and the insertion of an LST state in phase C to the right of the E-active state {PON}, respectively, within half switching period, T/2. Insertion of shoot-through states at these instants will not result in additional switching since, for example, the transition from {ONN} to {PNN} can be achieved by switching devices {Qa1,Qa2,Qa_1,Qa_2} from {OFF, ON, ON, OFF}through {ON, ON, ON, OFF} to {ON, ON, OFF, OFF} [47]. The process is reversed in the remaining half switching period. The phase A voltage during the UST state is the same as that of the "O" state because during the UST state, the voltage E is dropped across inductor L1 and the voltage seen by phase leg A is 0 V [see Fig. 3(b)]. Hence, the {UNN} and {ONN} states can supplement each other for voltage boosting without modifying the line-to-line volt–second average (normalized by taking the boost factor into account).

Applying the same analysis and moving on to the second transition ({PNN} to {PON}), where phase B switches from the "N" state to the "O" state, no shoot-through state is inserted (note that it is not possible to introduce UST or LST for the {PON} state for the reasons discussed earlier).Moving forward again to the third transition ({PON} to {POO}) where phase C switches from the "N" state to the "O" state, an LST state is inserted since the switching of devices {Qc1,Qc2,Qc_1,Qc_2} from {OFF, OFF, ON, ON} through {OFF, ON, ON, ON} to {OFF, ON, ON, OFF} will not affect phases A and B, which remain clamped to points P and O. The phase C voltage during the LST state is equal to that of the "O" state since the voltage E is dropped across inductor L2 and the voltage seen by phase C is 0 V [see Fig. 3(c)]. This means that the {POL} and {POO} states can supplement each other for voltage boosting without modifying the produced volt–second average (normalized by taking the boost factor into account).

TABLE IV
SWITCHING SEQUENCES AND INSERTION OF SHOOT-THROUGH STATES IN TRIANGLES 2–4

Triangle	Switching Sequence
2a	{ONN} → {UNN} → {OON} → {PON} → {POL} → {POO}
2b	{PPO} → {PPL} → {POO} → {PON} → {UON} → {OON}
3	{ONN} → {UNN} → {PNN} → {PON} → {POL} → {POO}
4	{OON} → {UON} → {PON} → {PPN} → {PPL} → {PPO}

When the previous methodology is applied to another distinct triangle, triangle 2a, a similar state sequence is derived and shown in Fig. 5(b). It is noted that although it is possible to insert a UST state at the ({OON} to {PON}) transition, no shoot-though state is inserted at this transition since doing so will result in an inferior output voltage. From the above, it is noted that in all triangles, the UST (or LST) states are inserted at the "E-Null" to "E-Active" state transitions with no shoot through states inserted at the "E-Active" to "E-Active" state transitions.

It is also noted that the shoot-through states do not affect the PWM control of the inverter, because they equivalently produce the same zero voltage at the load terminals. Another feature noted with the ULST modulation scheme is that the UST and LST states are introduced for only half of the total shoot-through duration of T_{ULST}, unlike the FST modulation scheme, where the Z-source network is shorted for the full shoot-through duration. Therefore, to produce the same boost factor for the ULST and FST schemes, we need to set $T_{ULST}/T = 2T_{FST}/T$, where T_{FST} is the FST duration. The available shoot-through period is limited by the E-null period that is determined by the modulation index according to (21) for the simple boost control method [34], [44]

$$\frac{T_{\mathrm{ULST}}}{2T} = \frac{T_{\mathrm{FST}}}{T} = \frac{T_U}{T} = \frac{T_L}{T} = 1 - M. \qquad (21)$$

Table IV gives a summary of the above discussions when the reference vector is in the various triangles of sector 1. A similar situation happens in sectors 2–6. However, it should be noted that in triangle 1, no shoot-through states are inserted because this corresponds to a low modulation index which causes the inverter to degenerate into three-level line-to-line voltage switching with no additional voltage boost produced [34].

V. SIMULATION RESULTS

To verify the proposed approach, simulations were first performed in SABER before the proposed SVM-based modulation algorithm was validated experimentally using an REC Z-source NPC inverter prototype. The hardware Z-source network was implemented using 6.3-mH inductors and 2200-μF capacitors, and powered by a 120-V split dc supply. The dc-link output of the Z-source network was connected to an existing NPC inverter to generate the expected five-level output line-to-line voltage waveform. The Z-source converter was controlled using a Texas Instrument TI6713 DSK and an Actel ProAsic 3 based field-programmable gate array board designed by the University of Nottingham. A switching frequency of 5 kHz was used for this study.

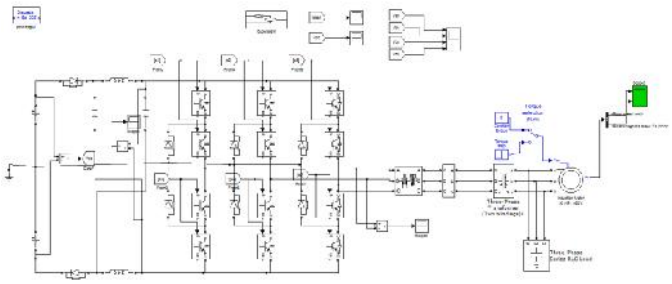
In this simulation platform, a standalone three-phase induction motor was used to verify the theoretical findings. To demonstrate the boosting ability of the REC Z-source NPC inverter, first, a modulation index,M of 0.825 and a shootthrough ratio, T_{ULST}/T of 0 were used for the non boost case. Fig. 6 shows the spectrum of the output line-to-line voltage, the output line-to-line voltage, line currents, Z-source capacitor voltage, and the dc-link voltage seen at the input of the NPC circuitry. The inverter dc-link voltage is obviously not boosted and the peak value of the output line-to-line voltage is maintained at almost 400V by the dc source. The spectrum of the output line to line voltage shows a peak fundamental component of 80 V, corresponding to a phase voltage of 47 V which is the expected value according to (16). High-quality

sinusoidal line currents are also observed. The voltage across the Z-source capacitors (VC1 , VC2 = VC) is clearly maintained at almost 120 V since no boosting is commanded. Similarly, the dc-link voltage seen by the NPC circuitry, Vi is maintained at around 120 V.

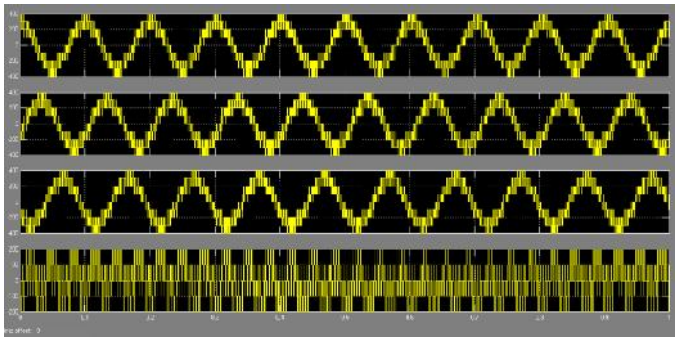
TABLE V
COMPARISON OF ULST AND FST STRATEGIES

	ULST strategy	Minimal loss FST strategy	Simplest FST strategy
THD	37.25%	58.75%	58.75%
Commutation count	2	4	4
Switching loss	Low	Medium	High

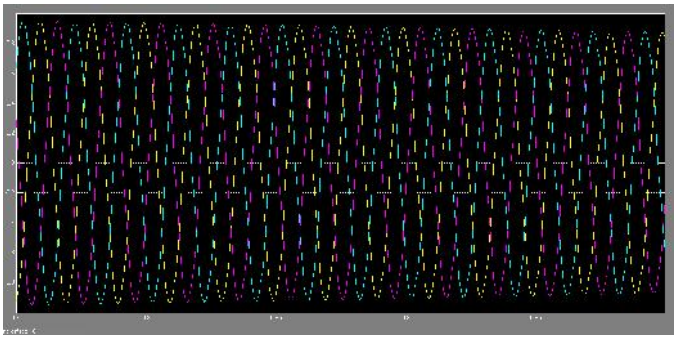
simulation results show that the REC Z-source NPC inverter, with the proposed SVM algorithm, is able to boost the output line-to-line voltage to a value higher than the available dc supply voltage with sinusoidal output currents. To show the improved harmonic performance of the ULST strategy over the FST strategy, simulations using the FST strategy were also carried out with the same parameters as those of the ULST strategy (except that $T_{FST}/T = 0.175 = 0.35/2$) and the results shown in Fig. 8. Table V gives a comparison of the performances of the ULST strategy, nonminimal loss FST, and the minimal loss FST strategies. Also, to show that the UST and LST states do not introduce any significant harmonic distortion to the output line-to-line voltage, the same dc-link voltage was used for the non boost mode (i.e., 2E = 120 V, $T_{ULST}/T = 0$) and the boost mode (2E = 120/1.53 V, $T_{ULST}/T = 0.35$) and their harmonic performances compared as shown in Fig. 9. Finally, the simulation results of the carrier-based PWM described in [36] using the same parameters as those of the proposed SVM strategy are shown in Figs. 10 and 11, and the total harmonic distortion (THD) of the output line-to-line voltage is compared to that of the proposed SVM strategy in Table VI.



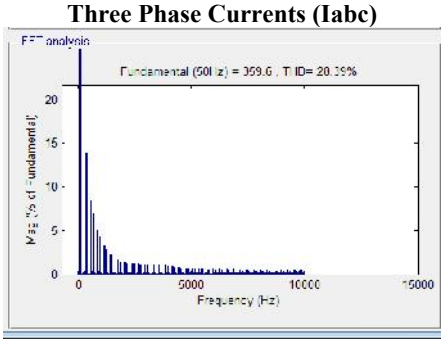
Simulink model for ULST based Induction Motor



Three Phase Voltages Vab,Vbc,Vca & phase to neutral voltage Van



Three Phase Currents (Iabc)



Voltage THD in %

From Table VI, it can be concluded that the harmonic performance of the proposed SVM strategy is comparable to the carrier-based PWM with zero-sequence voltage injection

TABLE VI
COMPARISON OF THD OF THE PROPOSED SVM AND CARRIER-BASED PWM WITH ZERO-SEQUENCE VOLTAGE INJECTION

	Proposed SVM	Optimised carrier-based PWM
Non boost Mode	37.77%	37.47%
ULST Mode	37.26%	36.81%

strategy described in [36] and hence is a competitive alternative for modulating the Z-source NPC inverter.

VI. CONCLUSION

In this paper, The simulation of Three level multilevel inverter is carried out in MATLAB/ Simulink, to identify the suitable level inverter which has comparatively less total harmonic distortion in its output. A comparative study is done for better configuration of multilevel inverter. a modified SVM for an REC Z-source NPC inverter is presented. The insertion of the shoottthrough states was such that the number of device commutations was kept at a minimum of six per sampling period, similar to that needed by a traditional NPC inverter. The Z-Source multilevel inverters are mainly used as drive for induction motors, STATCOM, shunt active power filters, aero space and solar powered applications. Application of SVPWM technique, incorporating Neuro-Fuzzy controller for performance improvement in closed loop control and hardware implementation of closed loop control are some of the important future scope of the present work.

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