Design A Low Power eight-bit Reversible Parallel Binary Adder/Subtractor

G.Laksmi Bhavani and A.Kalpana

Abstract- Reversible Logic is becoming more and more prominent technology having its applications inLow Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing. Reversibility plays an important role when energy efficient computations are considered. In this paper, Reversible eight-bit Parallel proposed. In all the three design approaches, the full Adder and Subtractors are realized in a single unit as compared to only full Subtractor in the existing design. The performance analysis is verified using number reversible gates, Garbage input/outputs and Quantum Cost. It is observed that Reversible eight-bit Parallel Binary Adder/SubtractorBinary Adder/Subtractor with Design.

Keywords

Reversible Logic, Quantum Cost, Low Power, Reversible Parallel Binary Adder/Subtractor.

I.INTRODUCTION

A Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate. Each Reversible gate has a cost associated with it called Quantum cost. The Quantum cost of a Reversible gate is the number of 2*2 Reversible gates or Quantum logic gates required in designing. One of the most important features of a Reversible gate is its garbage output i.e., every input of the gate which is not used as input to other gate or as a primary output is called garbage output. Arithmetic circuits such as Adders, Subtractors, Multipliers and Dividers are the essential blocks of a Computing system. Dedicated Adder/Subtractor circuits are required in a number of Digital Signal Processing applications. Several designs for binary Adders and Subtractors are investigated based on Reversible logic. Minimization of the number of ReversiReversible gates, Quantum cost and garbage inputs/outputs are the focus of research in Reversible logic.

Reversible Gates

The simplest Reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate. There are many 3*3 Reversible gates such as F, TG, PG and TR gate. The Quantum Cost of 1*1 Reversible gates is zero, and Quantum Cost of 2*2 Reversible gates is one. Any Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V+ (V issquare root of NOT gate and V+ is its hermitian) and FG gate which is also known as CNOT gate. The V and V+ Quantum gates have the property given in the Equations 1, 2 and 3.

V * V = NOT …… (1)
V * V+ = V+ * V = I …….. (2)
V+ * V+ = NOT ……. (3)

The Quantum Cost of a Reversible gate is calculated by counting the number of V, V+ and CNOT gates.Thapliyal and Ranganathan [5] proposed the design of Reversible Binary Subtractor using TR Gate. The particular function like Binary Subtraction is implemented using TR gate effectively by reducingnumber of Reversible gates, Garbage outputs and Quantum Cost. Thapliyal and Ranganathan [6] presented a design of Reversible latches viz., D Latch, JK latch, T latch and SR latch that are optimized in terms of quantum cost, delay and garbage outputs.. Lihui Ni et al., [7] described general approach to construct the Reversible full adder and can be extended to a variety of Reversible fulladders with only two Reversible gates. Irina Hashmi and Hafiz Hasan Babu [8] designed an efficient reversible barrel shifter which is capable of left shift/rotate used for high speed ALU applications.

Robert Wille et al., [9] explored two techniques from irreversible equivalence checking applied in the reversible circuit domain. (i) Decision diagram Technique equivalence checking for quantum circuits and (ii) Boolean satifiability checking for garbage input/outputs. Noor Muhammed Nayeem et al., [10] presented designs of Reversible shift registers such as serial-in serial-out, serial-in parallel-out, parallel-in serial-out, parallel-in parallel-out and universal shift registers. Majid Mohammadi, Mohammad Eshghi et al., [11] proposed a synthesis method to realize a Reversible Binary Coded Decimal adder/subtractor circuit. Genetic algorithms and don't care concepts used to design and optimize all parts of a Binary Coded Decimal adder circuit in terms of number of garbage inputs/outputs and quantum cost.

II. Proposed Model

Half Adder/Subtractor

Reversible half Adder/Subtractor–Design III is implemented with three Reversible gates of which two are FG gates each having Quantum cost of one and a PG gate with Quantum cost four is as shown in the Figure 1. The numbers of Garbage outputs is two i.e., *g1* and *g2*, Garbage inputs are one denoted by logical *zero* and Quantum Cost is six.

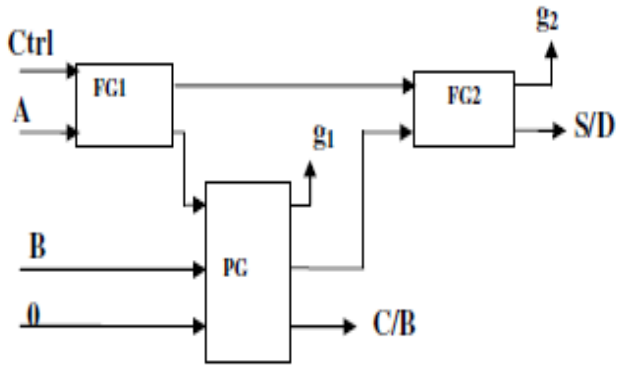

Figure1. Reversible Half Adder/Subtractor – Design

Full Adder/Subtractor

The Reversible Full Adder/Subtractor Design III consists of two FG, two PG gates, and their interconnections are shown

in the Figure2 . The three inputs are A, B, and Cin, The outputs are S/D and C/B. For Ctrl value *zero* the circuit performs addition and Subtraction for Ctrl value *one*. The numbers of Garbage inputs are 1 represented by logical *zero*. The Garbage outputs are 3 represented by *g1* to *g3*. The Quantum Cost for the design is 10. A Quantum Cost advantage of 11 is obtained
when compared to Adder/Subtractor Design I and of 4 when compared to Adder/Subtractor Design II. Quantum Cost advantage is due to the realization of Arithmetic blocks using two PG gates as against two F and one TR gate for Design I and two TR gates for Design II.

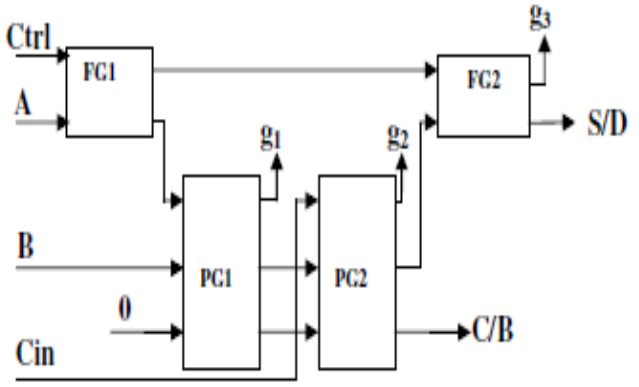

Figure2. Reversible Full Adder/Subtractor – Design

Reversible Eight-bit Parallel Binary Adder/Subtractor

The Half and Full Adder/Subtractor Design I, Design II and Design III are used to construct Reversible eight-bit Parallel Binary Adder/Subtractor is shown in the Figure3 . The ctrl input is used to differentiate eight-bit addition and subtraction functions. The two eight-bit binary numbers are A0 to A7 and B0 to B7. Carry/Borrow is obtained after Addition/Subtraction is represented by C_B1 to C_B7. The outputs Sum/Difference and Carry are shown as S_D0 to S_D7 and C_B8 respectively.

The implementation requires seven Full Adder/Subtractor units and one half Adder/Subtractor units in which first stage is half Adder/Subtractor.

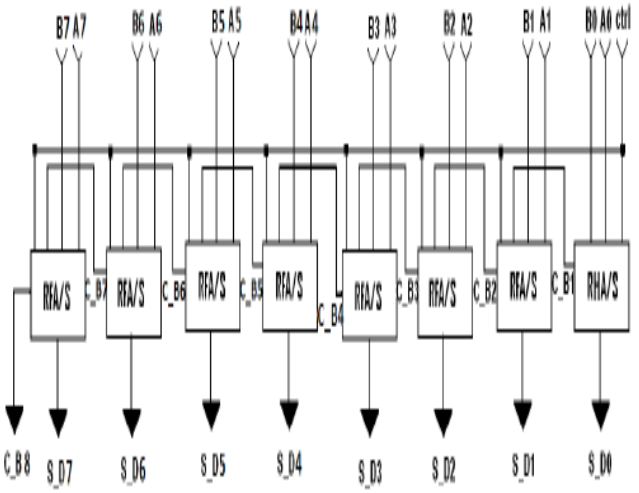

Figure3. Reversible Eight-bit parallel Binary Full Adder/Subtractor

III. Simulation Results

It is observed that Design III has better performance compared to Design II and Design I. The number of Reversible gates required for Design III is only 4 as compared to 8 and 4 in the cases of Design I and II respectively, which indicates that the improvement of 100% compared to Design I. The Garbage outputs are 5 in the case of Design I, whereas 3 in the case of Design II and Design III, i.e., the improvement is 65% in Design III compared to Design I. The Garbage inputs are 3 in the case of Design I and one in case of Design II and Design III, gives 200% improvement in Design III compared to Design I. Quantum Cost of Design III, Design II and Design I are 21, 14 and 10 respectively, resulting in improvement of Design III over Design II and Design I are 40% and 110% respectively.

The existing Reversible Binary Subtractor based on Reversible gate [5] to implement full Subtraction requires Quantum Cost of 12, Garbage inputs of *one* and Garbage outputs of *two*. The proposed Reversible eight-bit Parallel Binary Adder/Subtractor Design III is better compared to the existing design in terms of Quantum Cost, Garbage inputs and Garbage outputs and also in our design the Full Subtraction and Addition function is implemented together as compared to only Subtractor in the existing design. Hence we claim that Design III is better in terms of performance compared to theexisting designs.

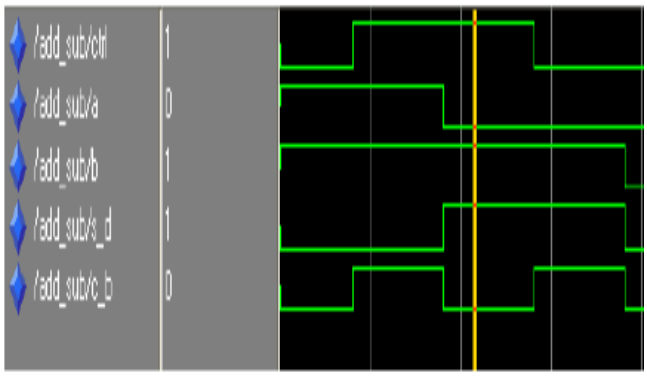

Figure4. Simulation result of Reversible Half Adder/Subtractor

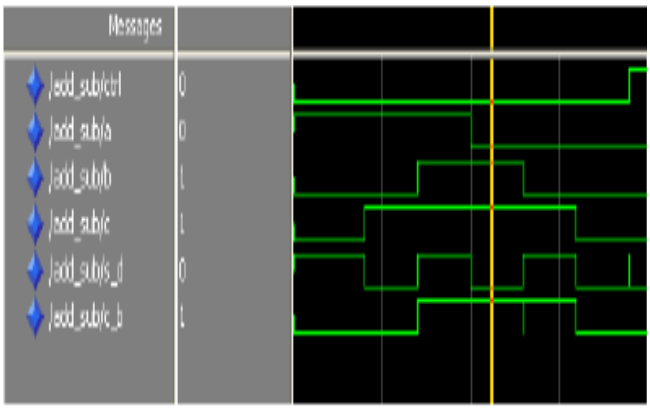

Figure5. Simulation result of Reversible Full Adder/Subtractor

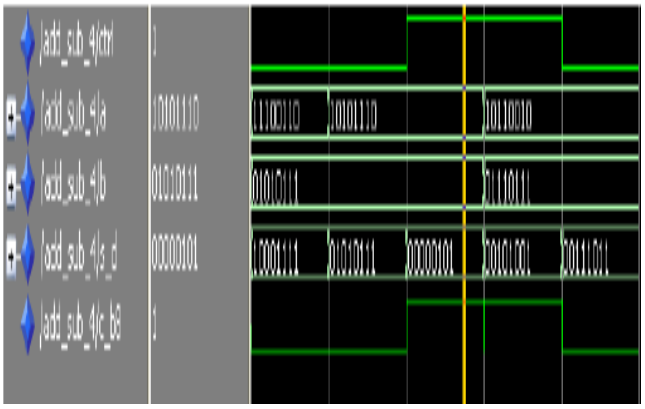

Figure6. Simulation result of Reversible eight-bit Parallel Binary Adder/Subtractor

Reversible Half, Full Adder/Subtractor and Reversible eight-bit Parallel Binary Adder/Subtractor with Design I, Design II and Design III are implemented using VHDL code and Simulated using Modelsim Simulator. The individual gate functionality is implemented using Behavioral style of Modeling, the overall logic is implemented using Structural style of Modeling and simulation results are shown in shown in Figure 4, 5 and 6.

Conclusions

The Reversible gates are used to implement Full Adder/Subtractor and Reversible eight-bit Parallel Binary Adder/Subtractor. In this paper, we proposed Reversible eight-bit Parallel Binary Adder/Subtractor unit. The Design used to implement half and full Adder/Subtractor. The Reversible eight-bit Parallel Binary Adder/Subtractor is built using three designs. The Design implementation of Reversible eight-bit Parallel Binary Adder/Subtractor has better performance as compared to Design I, Design II and existing design in terms of number of gates used, Garbage inputs/outputs and Quantum Cost, hence can be used for low power applications. The full Adder/Subtractor is implemented in a single unit in our design as compared to only full Subtractor in the existing design [5]. In future, the design can be extended to any number of bits for Parallel Binary Adder/Subtractor unit and also for low power Reversible ALUs, Multipliers and Dividers.

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