A Novel Approach to Power Optimized Memory Organization

By Using Multi-Bit Flip-Flops

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Abstract:

Power consumption is an important issue in modern high frequency and low power VLSI design. In modern VLSI designs, power consumed by clocking is taken as a major part of the design. Latches and flip-flops are the basic memory elements for storing information. In the proposed work, single-bit flip-flop for various applications is designed and its performance comparison over the multi-bit flip-flops is verified. One way to improve the flip-flop performance is to merge the clock pulse given to multiple flip-flops. Multi-bit flip-flop is designed by single clock pulse thereby maintaining the same functionality as that of two single-bit flip-flop. A serial-in serial-out shift register is designed using both Single- Bit Flip-Flop (SBFF) and Multi-B it Flip-Flop (MBFF) to compare its performance and it has been concluded from the comparison that the gate delay and net delay are reduced by using multi-bit flip-flops.

Index Terms: Clock power reduction, SBFF, MBFF, Merging, Shift register

I. INTRODUCTION

In latest years, the low power system has gained more importance because of the high requirement for portable electronic products. The numbers of components keep on increasing as technology enhances which leads to higher power density. Since the number of components increasing, dissipation of power is also increasing. This creates the necessity of power consumption reduction in order to improve the battery life and also evade overheating problem. Consequently, it has become a huge task for the designers to consider the power consumption in complex ICs. Moreover, power has become an important issue in modern VLSI design especially for those designs using deeply scaled CMOS technologies. Effective approaches have been projected to tackle this problem. Here an efficient approach named Multi-Bit Flip-Flop has been introduced to reduce the clock power consumption in which some flip flops are replaced by smaller amount of multi bit flip flops. When flip flops are reduced in number obviously number of clock sinks are reduced in clock tree synthesis which would lead to smaller power consumption.

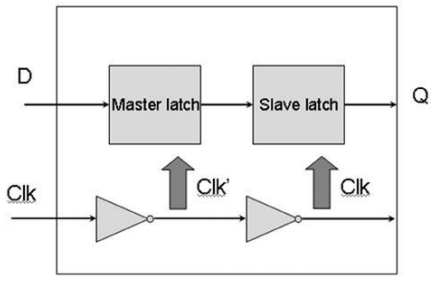


Fig. 1 Single bit flip-flop

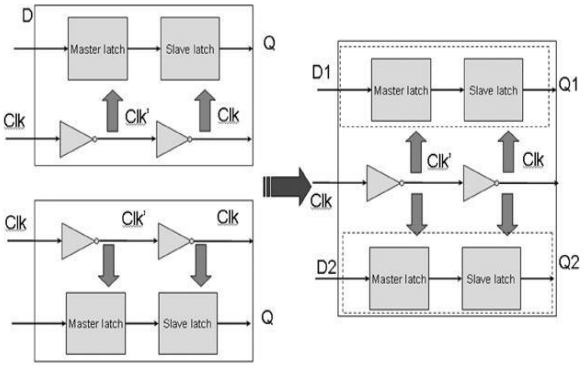


Fig. 2 merging two 1-bit flip-flops into one 2-bit flip-flop

Besides, device variations in the corresponding circuit can be reduced effectively when lesser flip flops are replaced by greater multi bit flip flops. Driving capability of the inverter based clock buffer increased expressively as CMOS technology advances. It indicates that several flip flops can share a common clock buffer to avoid wastage of power. Fig.2 shows the two 1-bit flip flops. Those flip flops are replaced by one 2-bit flip flop by sharing common clock buffer. It is shown in Fig.2. Since we perform replacement of flip flops, locations of some flip flops would be changed. It results in change in wire lengths of nets connecting pins to a flip-flop. The restriction of wire lengths of nets connecting pins to a flip-flop that cannot be longer than specified values after this process should be performed in order to avoid the violation of timing constraints. Area capacity of the region also considered here to assure that a new flip-flop can be placed within the preferred region. Two flip-flops of 1-bit are replaced by one flip-flop of 2-bit that is f1 and f2 are replaced by f3. It results in change in wire lengths of nets net, net2, net3, and net4.After replacement, the Manhattan distance of new nets net1, net2, net3, and net4 cannot be longer than the specified values to avoid the timing violation. The entire placement region is divided into numerous bins, and each bin has an area capacity denoting the remaining area that extra cells can be placed within it. Consider the area of *f*3 is 7. It is assigned to be placed in the same bin as *f*1. Since the remaining area of the bin is smaller than the area of *f*3, we cannot place *f*3 in that bin. It is also required to check the accessibility of new flip flops in the cell library. For example, when we wish to replace 2 and 3 bit flip-flops by a 5 bit flip-flop we have to check the availability of a 5 bit flip-flop in the cell library.

II. IMPLEMENTATION OF ALGORITHM

This algorithm has three effective consecutive steps to handle the power reduction problem. In first step transformation of coordinate system of cells is performed in order to identify what are the flip-flops can be merged. Building a combination table is done in the second step which avoids the wasting of time in finding impossible combination of flip-flops. In the third step of flip-flop replacement, in order to reduce the complexity whole chip region is partitioned into several sub-regions then flip-flop replacement is performed. Fig. 3 depicts this flow.

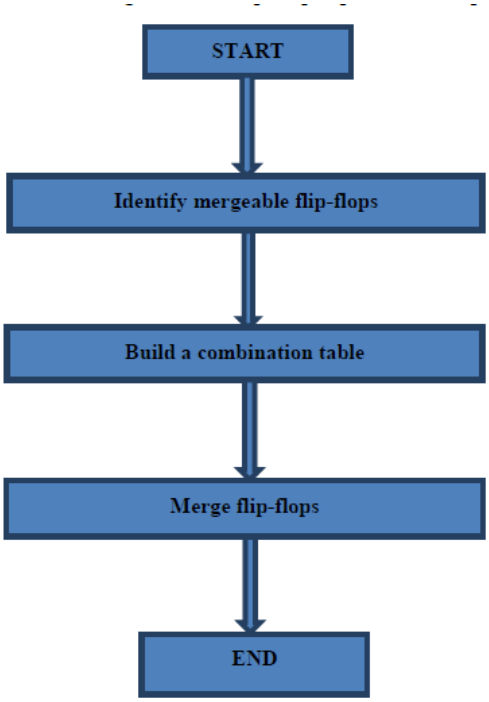


Fig. 3 Flow of algorithm

A. Sequential Circuits

Counters and registers belong to the category of MSI sequential logic circuits. A register is just a circuit with two or more D flip-flops connected together in such a way that they all work exactly the same way and are synchronized by the same clock and enable signals. Each flip-

flop in the group is used to store a different bit of the data. Registers are made more versatile by adding extra functionalities, such as counting and shifting. A shift register is a digital device used for storage and transfer of data. The basic building block in all shift registers is the flip-flop, mainly a D-type flip-flop. The storage capacity of a shift register equals the number of flip-flops used. The main usage for a shift register is for converting from a serial data input stream to a parallel data output or vice versa. A esign methodology for logic optimization with MBFFs. Such methodology creates the models of multi-bit registers in a cell library which can be inferred by existing logic synthesis tools. Based on the multi-bit register inference, it is possible to map a register-transfer level design directly to a gate level design with multi-bit register cells during logic synthesis. Similarly, register banking in a power-aware placement to build a low-power clock tree. However, it is difficult for the usage of multi-bit flip–flops to evaluate the trade-offs among the objectives of power, timing and area at the early placement stage.

B. Single-Bit Flip-flop

Fig. 4 shows the basic structure of single-bit flip-flop. A single-bit flip-flop has two latches (Master latch and Slave latch). The latches need Clk and Clk` signals to perform operations, such as Figure 4 shows**.** Flip-flops are used in a variety of application circuits, such as frequency division, counting circuits, data storage and transfer circuits.

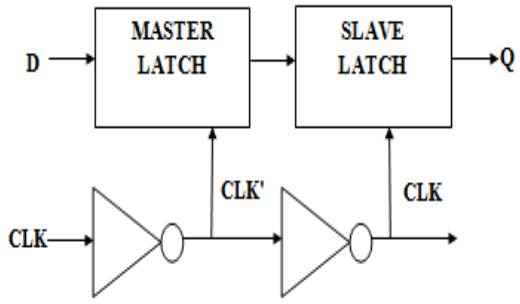


Fig. 4 Single-bit flip-flop

C. SISO Using Single-Bit Flip-Flop

The Fig. 5 shows an example of four-bit serial-in serial-out shift register using SBFF. The flip-flops shown respond to the LOW-to-HIGH transition of the clock pulses as indicated by their logic diagram. Initially, the contents of the shift register can be set to zero by means of the CLEAR line. During the first clock transition, ‘1’ is to the input of the first flip-flop, this ‘1’ is transferred to the output of flip-flop 1. The outputs of the other three flip-flops remain in the logic ‘0’ state as their D inputs were in the logic ‘0’ state at the time of clock transition. After four clock pulses this ‘1’ will be at the output of flip-flop 4. Thus, in a four-bit serial-in

serial-out shift register, it takes four clock cycles to load the data bits and another four cycles to read the data bits out of the register.

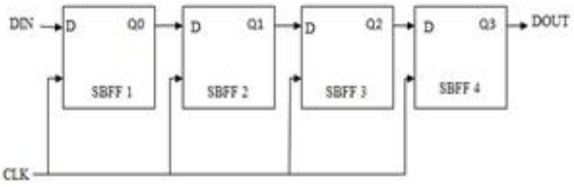
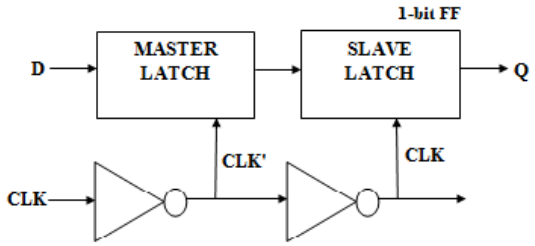


Fig. 5 SISO shift-register using single-bit flip-flop

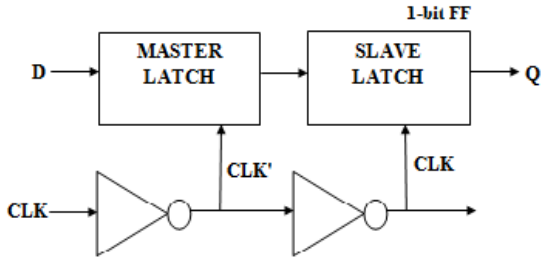
III. MULTI-BIT FLIP-FLOP METHODOLOGY

Fig. 6 shows the block diagrams of 1- and 2-bit flip-flops. The two 1-bit flip-flops as shown in Fig. 6(a) are replaced by the 2-bit flip-flop as shown in Fig. 6(b), the total power consumption can be reduced because the two 1- bit flip-flops can share the same clock buffer. Each 1-bit flip–flop contains two inverters, which generate opposite phase clock signals. Inside each 1-bit flip–flop, the master latch must receive the input signal from the connecting input pin and the slave-latch must send the output signal to the connecting output pin. As the process technology advances into nano- micro

process, even a minimum-sized inverter/buffer can still drive multiple flip-flops. Replacing several 1-bit flip-flops with one MBFF will significantly reduce the number of inverters. Consequently, the total power and area of the whole flipflops in a design are reduced.



6(a)



6(b)

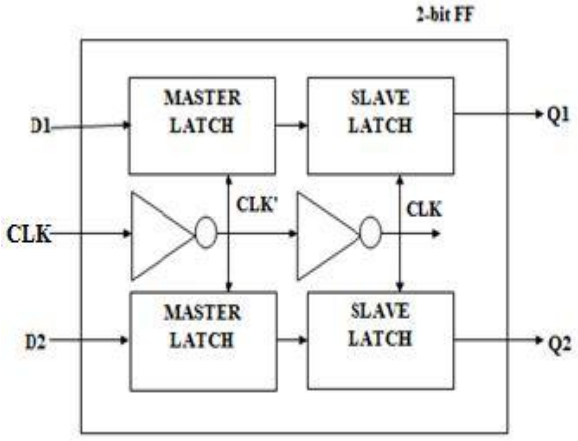


Fig. 6 Example of merging two 1-bit flip-flops into one 2-bit flip-flop.
(a) 1-bit flip-flops (before merging).
(b) 2-bit flip-flop (after merging).

A. Multi-Bit Flip-Flops

Fig. 7 shows the basic structure of multi-bit flip-flops. It takes multiple data input and results in multiple data output. Multi-bit flip-flop works same as single-bit flip-flop, during clock transition flip-flop latches all input to output and inactive state the flip-flop holds the data.

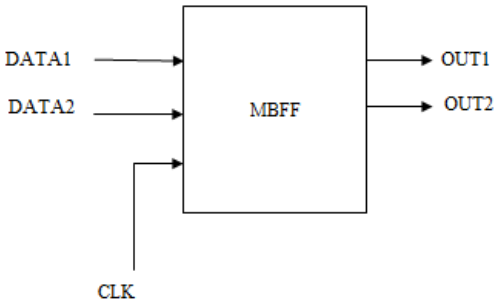


Fig. 7 Multi-bit flip-flops

According to [10] and [11], applying MBFFs may have the following advantages:
1) Eliminate some inverters and design area due to shared clock drivers and clock gating cells.
2) Less delay and power of the clock network due to fewer clock sinks.
3) Improved routing resource utilization especially when considering design for testability. The required routing resource for a scan chain is greatly reduced because of fewer cells in a scan chain.

B. SISO Implementation Using Multi-Bit Flip-Flops

The Fig. 8 shows the basic structure of serial- in serial-out shift register using MBFF. SISO shift register has five major Input / Output ports CLOCK, two data port as DIN 1 and DIN 2 respectively, and two output port as DOUT 1 and DOUT 2. Initially, the contents of the register can be set to zero by means of the CLEAR line. During the first clock pulses, ‘1’ and ‘0’ is to the input of the first flip flop, this ‘1’ and ‘0’ is transferred to the output of flip flop 1. After second clock pulses this ‘1’ and ‘0’ will be at the output of flip flop 2.

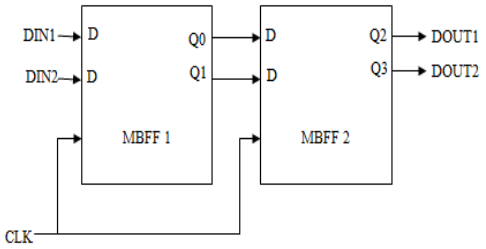


Fig. 8 SISO shift-register using multi-bit flip-flops

IV. EXPERIMENTAL RESULTS

This section shows our experimental results. The Single- Bit Flip-Flop and Multi-Bit Flip-Flops are successfully experimented using Xilinx ISE12.1 Simulator. The analysis of SISO designed using MBFF is targeted and verified on Xilinx FPGA of family Spartan-3E. The constraints taken to considerations are number of flip-flops used, clock buffer count and period analysis as Gate delay and Net delay. The number of flip-flops in SISO using SBFF is about half a number in SISO using MBFF.

A. Flip-Flops Clock Utilization

The below table I shows an experimental results of clock utilization.

TABLE I. SBFF AND MBFF CLOCK UTILIZATION

FLIP-FLOPS	NO OF CLOCK	CLOCK UTILIZATION
1-BIT	ONE	4%
2-BIT	TWO	8%
2-BIT(MULTI-BIT)	ONE	4%

B. Different Types of SISO Using SBFF and MBFF

The below table II shows an experimental results of various size of shift register using SBFF and MBFF.

TABLE II. COMPARISON OF SISO USING SBFF AND MBFF

SIZE		6-BIT		4-BIT		2-BIT	
NO OF FLIP- FLOP USED		6 (SBFF)	3 (MBFF)	4 (SBFF)	2 (MBFF)	2 (SBFF)	1 (MBFF)
CLOCK BUFFER		6	6	4	4	2	2
BEFORE CLOCK	GATE DELAY	2.798ns	2.660ns	2.716ns	2.576ns	2.576ns	2.549ns
	NET DELAY	0.669ns	0.531ns	0.587ns	0.447ns	0.447ns	0.420ns
AFTER CLOCK	GATE DELAY	4.283ns	4.283ns	4.283ns	4.283ns	4.283ns	4.283ns
	NET DELAY	0.420ns	0.420ns	0.420ns	0.420ns	0.420ns	0.420ns

C. RTL View of SISO Using Multi-Bit Flip-Flops

The below Fig. 9 shows the RTL view of Serial In Serial Out shift register using MBFF.

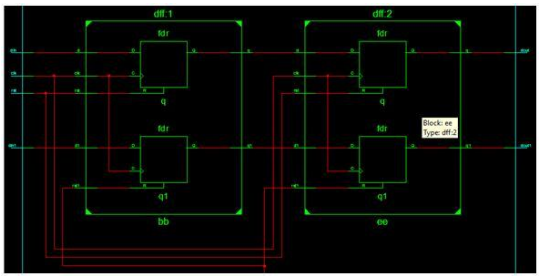


Fig. 9 RTL view of SISO using MBFF

D. Simulation Of SISO Using Multi-Bit Flip-Flops

The below Fig. 8 shows the simulation result of Serial In Serial Out shift register using MBFF.

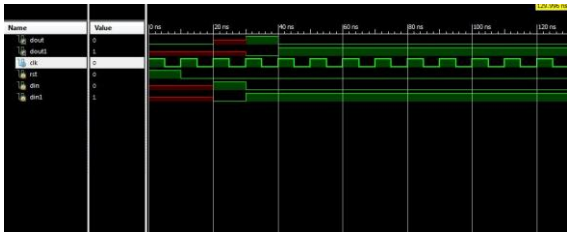


Fig. 10 Output waveform of SISO using MBFF

V. CONCLUSION

In this paper, we designed a single-bit flip-flop and multi-bit flip-flops. Various types of SISO shift register have been designed and synthesized using these flip-flops. The gate delay, net delay and clock buffer parameters in the design of

different SISO shift register using SBFF and MBFF are analyzed. Experimental results have shown that our approach is very effective in reducing not only flip-flop power consumption but also clock tree and Gate Delay and Net Delay when applying MBFFs to a sequential circuits design.

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