A Voltage Control Power Factor Correction Boost Converter with Phase Shifting Technique for Adjusting the Speed of BLDC Drive

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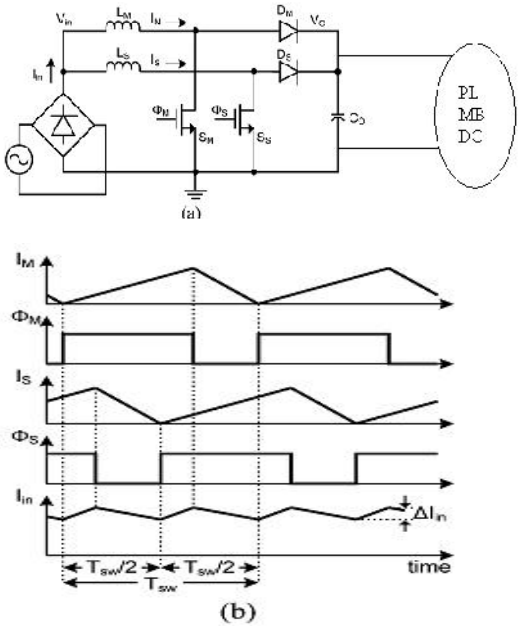
Abstract- In this paper, a buck half-bridge DC-DC converter is used as a single-stage power factor correction (PFC) converter for feeding a voltage source inverter (VSI) based permanent magnet brushless DC motor (PMBLDCM) drive. The front end of this PFC converter is a diode bridge rectifier (DBR) fed from single-phase AC mains. The PMBLDCM is used to drive a compressor load of an air conditioner through a three-phase VSI fed from a controlled DC link voltage. The speed of the compressor is controlled to achieve energy conservation using a concept of the voltage control at DC link proportional to the desired speed of the PMBLDCM. Therefore the VSI is operated only as electronic commutators of the PMBLDCM. The stator current of the PMBLDCM during step change of reference speed is controlled by a rate limiter for the reference voltage at DC link. The proposed PMBLDCM drive with voltage control based PFC converter is designed, modeled and its performance is simulated in Matlab-Simulink environment for an air conditioner compressor driven through a 1.5 kW, 1500 rpm *PMBLDC motor. The evaluation results of the proposed speed control scheme are presented to demonstrate an improved efficiency of the proposed drive system with PFC feature in wide range of the speed and an input AC voltage.*

Index Terms: PMBLDCM- permanent magnet brushless DC motor; voltage source inverter (VSI); diode bridge rectifier (DBR)

1. INTRODUCTION

In this project, a buck- boost half-bridge DC-DC converter isused as a single-stage power factor correction (PFC) converterfor feeding a voltage source inverter (VSI) based permanentmagnet brushless DC motor (PMBLDCM) drive. The front endof this PFC converter is a diode bridge rectifier (DBR) fed fromsingle-phase AC mains. The PMBLDCM is used to drive acompressor load of an air conditioner through a three-phaseVSI fed from a controlled DC link voltage. The speed of thecompressor is controlled to achieve energy conservation using aconcept of the voltage control at DC link proportional to thedesired speed of the PMBLDCM. Therefore the VSI is operatedonly as an electronic commutators of the PMBLDCM. The statorcurrent of the PMBLDCM during step change of referencespeed is controlled by a rate limiter for the reference voltage atDC link. The proposed PMBLDCM drive with voltage controlbased PFC converter is designed, modeled and its performanceis simulated in Matlab-Simulink environment for an airconditioner compressor driven through a 1.5 kW, 1500 rpmPMBLDC motor. The evaluation results of the proposed speedcontrol scheme are presented to demonstrate an improvedefficiency of the proposed drive system with PFC feature in widerange of the speed and an input AC voltage.



(a) Two-phase interleaved PFC boost converter with PLMBDC Drive and (b) waveforms of a two-phase interleaved CRM PFC converter.

The lower power handling capability of the DCM and CRM can be overcome by paralleling multiple converters [6]. Fig. 1(a) shows a simplified block diagram of a two-phase interleaved PFC boost converter. As shown in Fig. 1(b), if the switching signalsΦMandΦS of the two converters are exactly 180◦ out of phase, the rippleΔIin of the input current can be greatly reduced, which allows smaller input filter. For the DCM and CCM operation, it is easy to generate the switching signalsΦMand ΦSspaced by 180◦ because the switching frequencyfswis fixed. A clock signal whose frequency is 2×fsw is divided by 2 to get a 50% duty reference clock for switching signal generation. The rising and falling edges of the 50% duty reference clock are used to generate the switching signalsΦMandΦS, respectively, while ensuring 180◦ spacing between them. If a converter operates at the CRM, however, the switching frequency changes according to the instantaneous input line voltage and output current at every switching cycle; therefore, it is impossible to generate the 180◦ out of phase switching signals by the method explained previously.

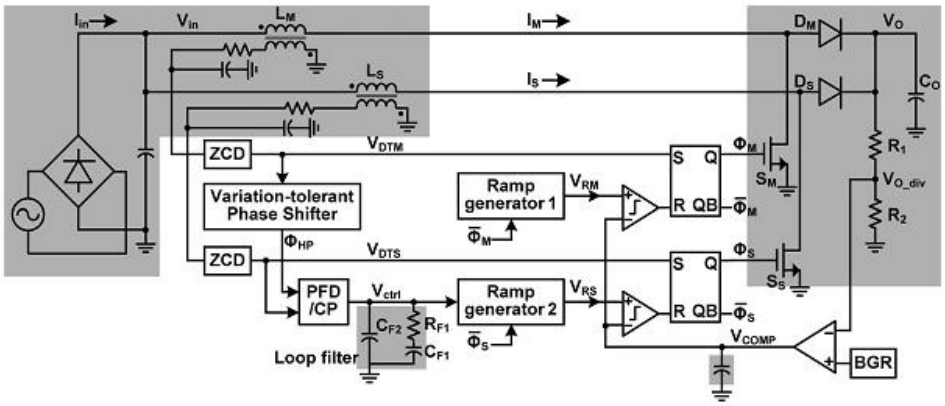


Fig. 2. Two-phase interleaved PFC boost converter with a VTPS. The components in the shaded regions are off-chip.

II. TWO-PHASEINTERLEAVEDCRM PFC BOOST CONVERTERWITH AVTPS

A. Architecture

Fig. 2 shows the block diagram of the two-phase interleaved PFC boost converter with the proposed VTPS operating at the CRM. The upper converter consisting ofLM,DM, and Smis the master and the lower one consisting ofLS,DS, andSSis the slave. The output voltage level is compared with the reference level generated by the bandgap reference (BGR) to generate the error voltageVCOMP. For the master converter, the fixed slope ramp signalVRMis compared with the error voltageVCOMPand the switching signal ΦMbecomes LOW whenVRMis larger than VCOMP, decreasing the inductor current IM. The voltage level of the secondary winding of the transformers is utilized to detect the zero current of the primary winding. The zero current detector (ZCD) generates the pulseVDTM, settingΦMto HIGH when the voltage level of the secondary winding is lower than the reference level. The operation of the slave converter is similar to that of the master except that the slope of the ramp signalVRSis variable to get the accurate 180◦ phase difference between the master and slave converters. The slope ofVRSis adjusted by the phase shifting loop consisting of the phase-frequency detector (PFD), charge pump (CP), loop filter, and ramp generator, so the rising edge of the ZCD outputVDTSof the slave converter is locked to that of ΦHPwhich is 180◦ phase shifted fromVDTMby the phase shifter. Because the switchSS of the slave converter is turned ON by the rising edge of VDTS, the turn-ON instant of the slave converter is 180◦ phase shifted from that of the master converter.

B. Stability of the Phase Shifting Loop With the VTPS

In the CRM PFC boost converter, the switching periodtsw is the sum of the on-timetonand off-timetoff of the switch and is given as

$$t_{\rm sw} = t_{\rm on} + t_{\rm off} = t_{\rm on} + \left(\frac{v_{\rm in}}{v_o - v_{\rm in}}\right) t_{\rm on} = \left(\frac{v_o}{v_o - v_{\rm in}}\right) t_{\rm on}$$

wherevin andvoutare input and output voltages, respectively. The variables in (4) can be represented as the sum of the dc value and small-signal variation component as

$$t_{\rm sw} = T_{\rm SW} + \hat{t}_{\rm sw}$$
$$t_{\rm on} = T_{\rm ON} + \hat{t}_{\rm on}$$
$$v_o = V_O + \hat{v}_o$$
$$v_{\rm in} = V_{\rm in} + \hat{v}_{\rm in}.$$

Permanentmagnet***Brushless*** Direct Current (BLDC) motors are one of the motor types rapidly gaining popularity. PMBLDC motors are used in industries such as Appliances, Automotive, Aerospace, Consumer, Medical, Industrial Automation Equipment and Instrumentation. As the name implies, PMBLDC motors do not use brushes for commutation; instead, they are electronically commutated. PMBLDC motors have many advantages over brushed DC motors and induction motors. A few of these are:• Better speed versus torque characteristics

- High dynamic response
- High efficiency
- Long operating life
- Noiseless operation
- Higher speed ranges

TABLE I
PERFORMANCE SUMMARY

Parameter	Value	Unit	Condition
Technology	0.35-µm BCDMOS process		
Operating mode	CRM		-
Input line voltage	90~264	V_{RMS}	AC
Output voltage	393	V	DC
Inductor value	160	µH	
Capacitor value	164	µF	
MOSFET	TK13A60D		
Diode	SFF1008G		
Minimum suppotable switching freqneucy	25	kHz	Frequency limitation of the phase shifter
Supply voltage	10~25	V	-
Reference voltage	3.7	V	-
Internal supply	5	V	Linear regulator output
Maximum output current	800	mA	Maximum output power : 320-W
Output buffer rising time	75	nsec	Load capacitance : 2-nF
Output buffer falling time	91	nsec	
Current consumption	6	mA	Excluding driving current of power switch
Quiescent current	0.12	mA	-

III. EXPERIMENTALRESULTS

In order to verify the performance of the proposed VTPS, three types of two-phase interleaved CRM PFC boost converter providing 320 W maximum output power have been implemented in a 0.35-µm BCDMOS process. The three converters have the same circuitry except the phase shifting network. Two of them have the conventional phase shifter, that is, the conventional one with the UP and DOWN current sources [7] and the one with the sample-and-hold circuit [8]. The third one has the proposed VTPS. Among the three converters, Fig. 3 shows the microphotograph of the one with the proposed phase shifter. The area of the whole chip is 2.65 mm^2 where the proposed phase shifter occupies 0.14 mm^2

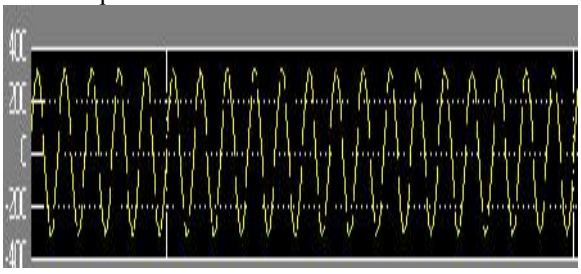


Fig 3.VSS Charcterstics

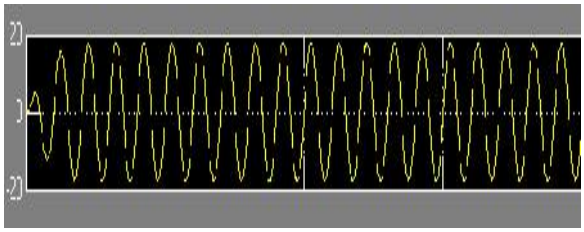


Fig 4.ISS Charcterstics

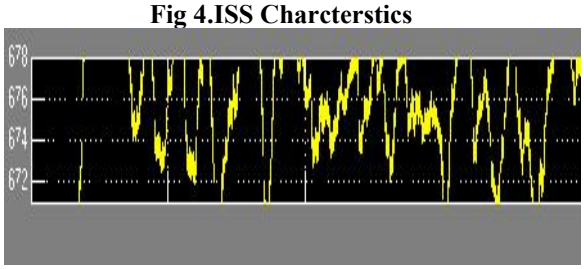


Fig 4.VDC Charcterstics

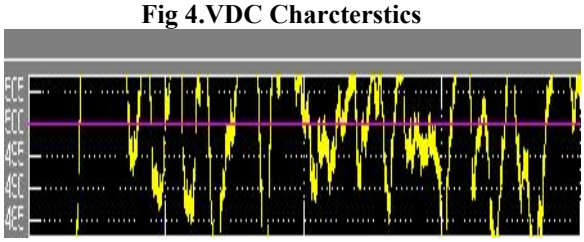


Fig 5 Speed Charcterstics

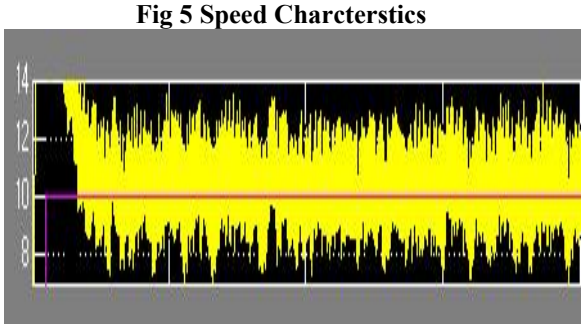


Fig 6 Torque Charcterstics

The harmonics are lower than the IEC 61000-3-2 Class-D specifications. The performance of the PFC boost converter employing the proposed VTPS is summarized in Table I.

IV. CONCLUSION

A new speed control strategy of a PMBLDCM drive is validated for a compressor load of an air conditioner which uses the reference speed as an equivalent reference voltage at DC link. The speed control is directly proportional to the voltage control at DC link. The rate limiter introduced in the reference voltage at DC link effectively limits the motor current within the desired value during the transient condition (starting and speed control). The additional PFC feature to the proposed drive ensures nearly unity PF in wide range of speed and input AC voltage. Moreover, power quality parameters of the proposed PMBLDCM drive are in conformity to an International standard IEC 61000-3-2. The proposed drive has demonstrated good speed control with energy efficient operation of the drive system in the wide range of speed and input AC voltage. The proposed drive has been found as a promising candidate for a PMBLDCM driving Air-Con load in 1-2 kW power range.

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