A New Inverter Topology for Common Mode Ground Leakage Current Elimination in Grid Connected PV Systems Using Virtual DC Bus Concept

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Abstract—In order to eliminate the common-mode (CM) leak-age current in the transformerless photovoltaic (PV) systems, the concept of the virtual dc bus is proposed in this paper. By con-necting the grid neutral line directly to the negative pole of the dc bus, the stray capacitance between the PV panels and the ground is bypassed. As a result, the CM ground leakage current can be suppressed completely. Meanwhile, the virtual dc bus is created to provide the negative voltage level for the negative ac grid current generation. Consequently, the required dc bus voltage is still the same as that of the full-bridge inverter. Based on this concept, a novel transformerless inverter topology is derived, in which the virtual dc bus is realized with the switched capacitor technology. It consists of only five power switches, two capacitors, and a single fil-ter inductor. Therefore, the power electronics cost can be curtailed. This advanced topology can be modulated with the unipolar sinu-soidal pulse width modulation (SPWM) and the double frequency SPWM to reduce the output current ripple. As a result, a smaller fil-ter inductor can be used to reduce the size and magnetic losses. The advantageous circuit performances of the proposed transformer-less topology are analyzed in detail, with the results verified by a 500-W prototype.

Index Terms—Common mode (CM) current, photovoltaic (PV) system, switched capacitor, transformerless inverter, unipolar si-nusoidal pulse width modulation (SPWM), virtual dc bus.

I.INTRODUCTION

The distributed photovoltaic (PV) power generation systems have received increasing popularity in both the com-mercial and residential areas [1]–[3]. In most occasions, the inverters are used to feed the PV power into the utility grid. It is important for the PV inverter to be of high efficiency, due to the relatively high price of the PV panels [4], [5]. Small size is also strongly desired for the low-power and single-phase systems, especially when the inverters are installed indoor.

Based on the virtual dc bus concept, a novel inverter topology is derived as an example to show the clear advantages of the proposed methodology, which is shown in Fig. 7. It consists of five power switches S_1 –S_5 and only one single filter inductor L_f .The PV panels and capacitor C_1 form the real dc bus while the virtual dc bus is provided by C_2 . With the switched capacitor technology, C_2 is charged by the real dc bus through S_1 and S_3 to maintain a constant voltage. This topology can be modulated with the unipolar SPWM and double-frequency SPWM. The detailed analysis is introduced as follows.

In the traditional grid-connected PV inverters, either a line-frequency or a high-frequency transformer is utilized to provide a galvanic isolation between the grid and the PV panels. Re-moving the isolation transformer can be an effective solution to increase the efficiency and reduce the size and cost [6]. How-ever, if the transformer is omitted, the common-mode (CM) ground ***leakage*** current may appear on the parasitic capacitor between the PV panels and the ground [7], [8]. The existence of the CM current may reduce the power conversion efficiency, increase the grid current distortion, deteriorate the electric mag-netic compatibility, and more importantly.

The CM current path in the grid-connected transformerless PV inverter system is illustrated in Fig. 1. It is formed by the power switches, filters, ground impedance Z_G , and the para-sitic capacitance C_{PV} between the PV panels and the ground. According to [10], the CM current path is equivalent to an *LC* resonant circuit in series with the CM voltage.

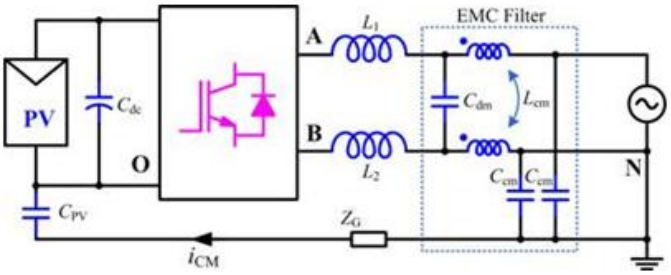

Fig. 1. CM current path for the transformerless PV inverter

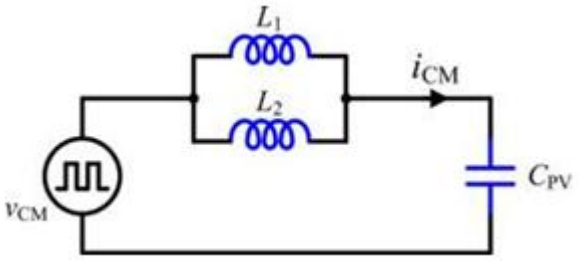

Fig. 2. Equivalent circuit for the CM current path

combine cells of different voltage ratings [5], [6], different topologies], or even combine switch converters.

If the switching action of the inverter generates high-frequency CM voltage, the CM current $i_{C\,M}$ may be exited on the *LC* circuit. From this point of view, the topology and modulation strategy adopted for the transformerless PV power system should guarantee that $v_{C\,M}$ is constant or only varies at low frequency, such as 50 Hz/60 Hz line frequency.

A simple way to realize this goal is to use the full-bridge inverter with the bipolar sinusoidal pulse width modulation (SPWM), of which the CM voltage is fixed at half the dc bus volt-age. Comparing with the bipolar SPWM, the unipolar SPWM has better performance in terms of the output current ripple and switching losses, but cannot be directly used for the full-bridge inverter in the transformerless application, because it generates the switching frequency CM voltage.

For this reason, some state-of-the-art topologies, such as the H5 inverter, the HERIC inverter, etc., have been developed based on the full-bridge inverter, to keep $v_{C\,M}$ constant when the unipo-lar modulation is used [11]–[16]. Some of these topologies are exhibited in Fig. 3. By inserting extra switches into the full-bridge inverter either on the dc or ac side, the dc bus can be disconnected from the grid when the inverter output voltage is at zero voltage level, so that the CM current path is cut off.

Such solutions need two filter inductors with independent iron cores, which may lead to a rise in the size and cost. Moreover, the dc and ac sides cannot be perfectly disconnected by the power switch because of the switch parasitic capacitance, so the CM current may still exist [10].

Another kind of solution is to use the half-bridge inverter with the grid neutral line directly connected to the midpoint of the dc bus, as shown in Fig. 4. In this way, the voltage across the parasitic capacitor is clamped to be constant by the dc bus capacitor. However, this method has an important disadvantage that the required dc bus voltage should be doubled compared with the full-bridge topologies. For the 220 V_{ac} system, it can be as high as 700 V. Although the three-level neutral point clamped (NPC) circuit can help improve the performance of the half-bridge inverter, the dc bus voltage is still high [17], [18].

Besides the aforementioned classic circuits, there are other topologies proposed in recent literature works, some of which are listed in Fig. 5. The Karschny inverter [19] and the paralleled-buck inverter [20] are derived from the buck–boost and buck circuits, respectively. These solutions have high reliability, but are not capable of supplying the reactive power to the grid. The inverter proposed in [21] employs a capacitor voltage divider to keep the CM voltage constant, but is regarded to be of higher conduction losses.

In this paper, a novel topology generation strategy called the virtual dc bus concept is proposed for the transformerless grid-connected PV inverter. In this solution, the grid neutral line is connected directly to the negative pole of the dc bus, so that the voltage across the parasitic capacitor is clamped to zero. As a result, the CM current is eliminated completely. Meanwhile, the virtual dc bus is created to help generate the negative output voltage. The required dc bus voltage is still the same as the full-bridge, and there is not any limitation on the modulation strategy since the CM current is removed naturally by the circuit
structure. In this way, the advantages of the full-bridge- and half-bridge-based solutions are combined together.

Based on the aforementioned innovative idea, a novel in-verter topology is proposed with the virtual dc bus concept by employing the switched capacitor technology. The proposed in-verter can be modulated with the unipolar SPWM and double frequency SPWM. It consists of only five power switches and a single filter inductor, so the cost of the semiconductor and magnetic components can be reduced.
This paper is organized as follows. The virtual dc bus concept is explained in Section II. Based on it, a novel inverter topology with the switched capacitor is derived in Section III, and the modulation strategy and operation principle are described in detail. The current stress caused by the operation of the switched capacitor is analyzed in Section IV. The circuit performance is evaluated in Section V. The experimental results of a 500-W prototype with 20 kHz switching frequency are given in Section VI to verify the analysis. A summary is given in the final section.

II. VIRTUAL DC BUS CONCEPT

The concept of the virtual dc bus is depicted in Fig. 6. By connecting the grid neutral line directly to the negative pole of the PV panel, the voltage across the parasitic capacitance C_{PV} is clamped to zero. This prevents any leakage current flowing through it.
With respect to the ground point N, the voltage at midpoint B is either zero or $+V_{dc}$, according to the state of the switch bridge. The purpose of introducing the virtual dc bus is to generate the negative output voltage, which is necessary for the operation of the inverter. If a proper method is designed to transfer the energy between the real bus and the virtual bus, the voltage across the virtual bus can be kept the same as the real one. As shown in Fig. 6, the positive pole of the virtual bus is connected to the ground point N, so that the voltage at the midpoint C is either zero or $-V_{dc}$. The dotted line in the figure indicates that this connection may be realized directly by a wire or indirectly by a power switch. With points B and C joined together by a smart selecting switch, the voltage at point A can be of three different voltage levels, namely $+V_{dc}$, zero, and $-V_{dc}$.

Since the CM current is eliminated naturally by the structure of the circuit, there is not any limitation on the modulation strat-egy, which means that the advanced modulation technologies such as the unipolar SPWM or the double-frequency SPWM can be used to satisfy various PV applications.

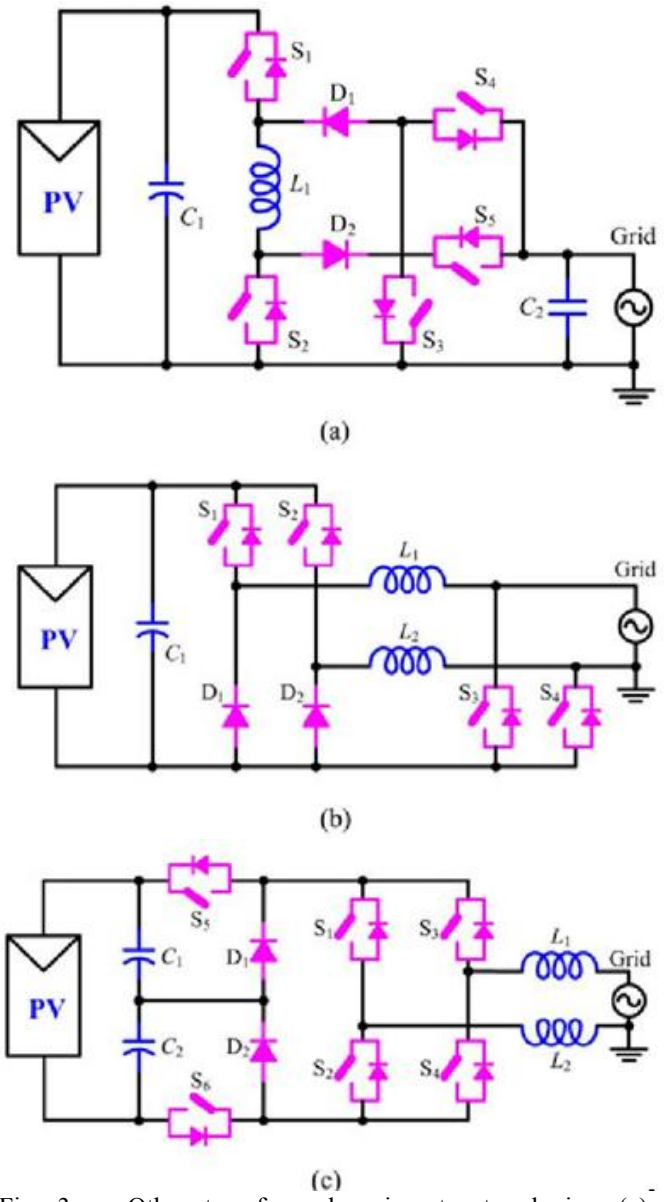

Fig. 3. Other transformerless inverter topologies: (a) Karschny inverter [19];(b) paralleled-buck inverter [20]; (c) H6 inverter with capacitor voltage divider [21]

III. TOPOLOGY AND MODULATION STRATEGY

Based on the virtual dc bus concept, a novel inverter topology is derived as an example to show the clear advantages of the proposed methodology, which is shown in Fig. 7. It consists of five power switches S_1 –S_5 and only one single filter inductor L_f. The PV panels and capacitor C_1 form the real dc bus while the virtual dc bus is provided by C_2. With the switched capacitor technology, C_2 is charged by the real dc bus through S_1 and S_3 to maintain a constant voltage. This topology can be modulated with the unipolar SPWM and double-frequency SPWM. The detailed analysis is introduced as follows.

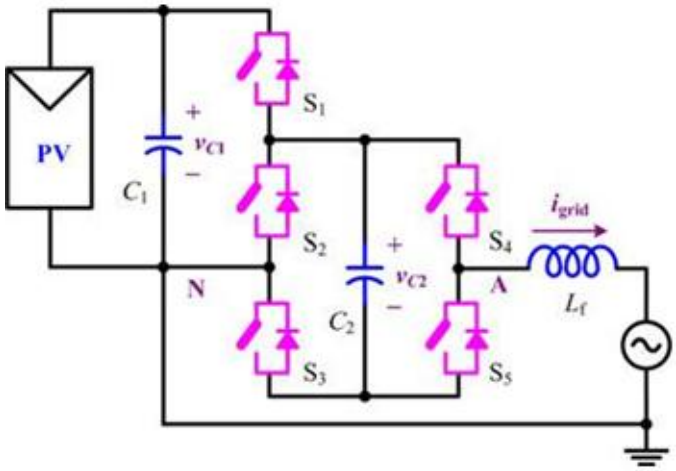

Fig. 4. Proposed topology.

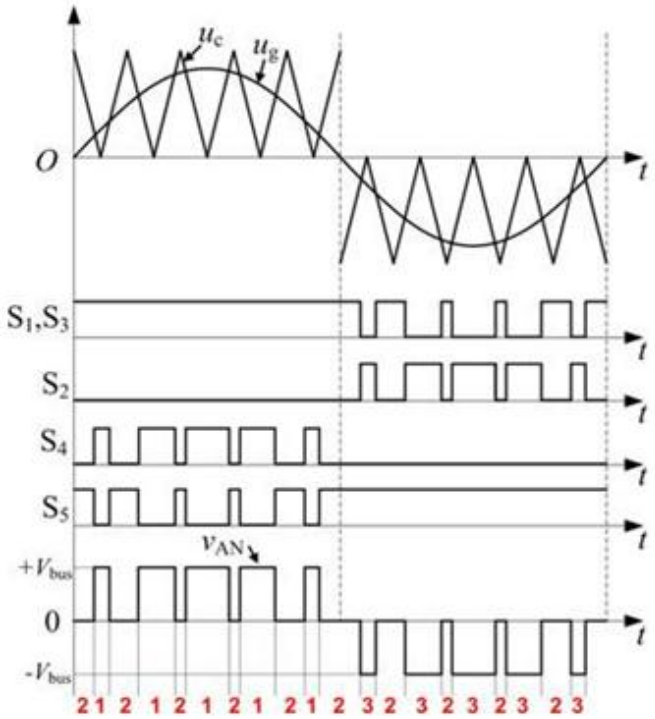

Fig. 5. Unipolar SPWM for the proposed topology.

The waveform for the unipolar SPWM of the proposed in-verter is displayed in Fig. 8. The gate drive signals for the power switches are generated according to the relative value of the modulation wave u_g and the carrier wave u_c. During the positive half grid cycle, $u_g > 0$. S_1 and S_3 are turned ON and S_2 is turned OFF, while S_4 and S_5 commutate complementally with the car-rier frequency. The capacitors C_1 and C_2 are in parallel and the circuit rotates between states 1 and 2 as shown in Fig. 10.

During the negative half cycle, $u_g < 0$. S_5 is turned ON and S_4 is turned OFF. S_1 and S_3 commutate with the carrier frequency synchronously and S_2 commutates in complement to them. The circuit rotates between states 3 and 2. At state 3, S_1 and S_3 are turned OFF while S_2 is turned ON. The negative voltage is generated by the virtual dc bus C_2 and the inverter output is at negative voltage level. At state 2, S_1 and S_3 are turned ON while S_2 is turned OFF. The inverter output voltage $v_{A\,N}$

equals zero; meanwhile, C_2 is charged by the dc bus through S_1 and S_3 .

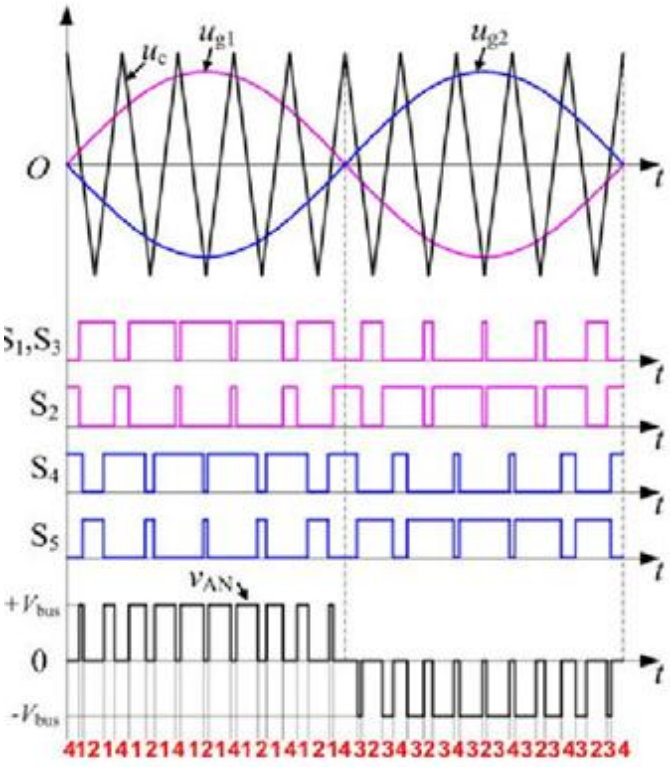

Fig. 6. Double SPWM for the proposed topology

The proposed topology can also work with double-frequency SPWM to achieve a higher equivalent switching frequency, as shown in Fig. 9. In the double-frequency SPWM, the five power switches are separated into two parts, and are modu-lated with two inverse sinusoidal waves respectively. S_1 , S_2 , and S_3 are modulated with u_{g1} , while S_4 and S_5 are modulated with u_{g2} .

During the positive half grid cycle, the circuit rotates in the sequence of "state 4 – state 1 – state 2 – state 1," and the output voltage $v_{A\,N}$ varies between $+V_{dc}$ and the zero with twice of the carrier frequency. During the negative half grid cycle, the circuit rotates in the sequence of "state 4 – state 3 – state 2 – state 3," and the output voltage $v_{A\,N}$ varies between $-V_{dc}$ and zero.

Under the same switching frequency, the output voltage wave-forms of the proposed circuit and the H5 circuit are identical to each other. This results in similar output current ripple and magnetic losses, if the same filter inductor configurations are used. Nevertheless, the H5 circuit has to employ two inductors with separated iron cores, while the proposed circuit only needs one. This may lead to a reduction in the size of the iron core, although the total inductor value is still the same.

As for the proposed topology, the stray capacitance between the PV panels and the ground is directly bypassed. Due to the configuration of the virtual dc bus, the CM current is eliminated completely.

In conclusion, the conduction and switching losses in the power devices of the proposed topology are quite similar to those of the H5 circuit. The main drawback is that larger capacitors are needed to reduce the ESR losses in the capacitor and ensure their life time. This issue can be alleviated by adding a thin film capacitor in parallel to the aluminum electrolyte one to absorb the high-frequency pulsating current. Fortunately, the clear advantage of the proposed topology is that it has better performance in eliminating the CM current. The solution with virtual dc bus concept provides a new idea for developing the transformerless inverter for the PV applications.

IV. EXPERIMENTAL RESULTS

A 500-W prototype is built to verify the functionality of the proposed topology and the idea of the virtual dc bus concept. The terminal voltage for a 500-W PV panel is typically 40–60 V. The high step-up converter proposed in [24] can be used to acquire the 400 V dc bus. Since the input and output terminals of the step-up converter share a common ground, the grid neutral line is still connected to the negative pole of the PV panel. Therefore, the front-end high step-up converter does not affect the elimination of the CM current for the proposed topology.

Since the voltage across C_2 is not completely symmetrical during the positive and negative half cycle for the proposed topology, the dc current elimination algorism is required to limit the dc current injected into the grid. The measured dc bias of i_{grid} is below 10 mA for the prototype, which is less than 0.5% of the rated output current. This is in accordance with the IEEE 1547 standard for interconnecting distributed resources with the power system.

To verify the reactive power capability of the proposed circuit, a simulation waveform is exhibited in Fig. 18, in which the power factor is set at 0.94. With this characteristic, the proposed circuit is able to adjust the reactive power to help regulate the grid voltage.

The current stress on S_3 is shown in Fig. 19. The extra cur-rent stress only appears in the negative half cycle and the peak current on S_3 is approximately $4I_m$.

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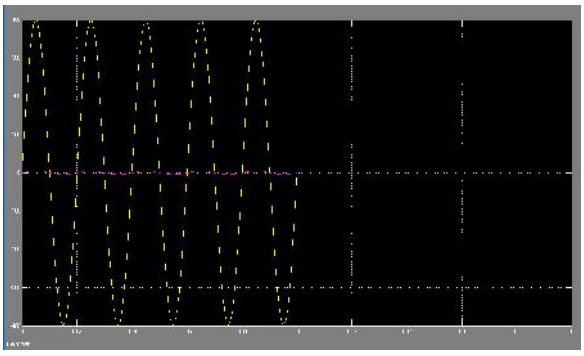

Fig : Simulation waveform for active power generation

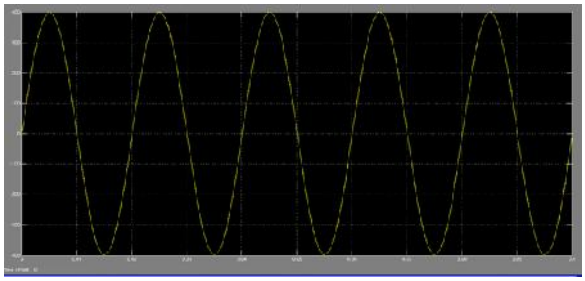

Fig : Simulation waveform for Output current and grid voltage

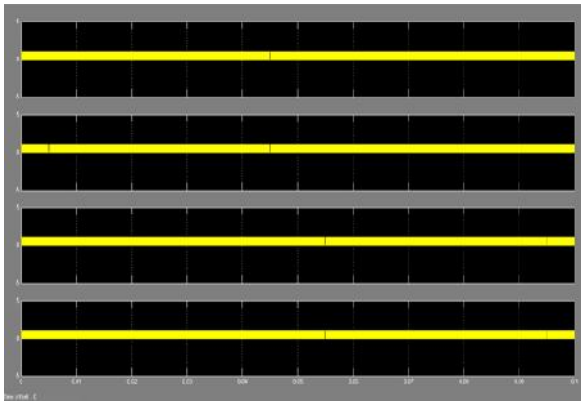

Fig : Simulation waveform Current harmonics reduction

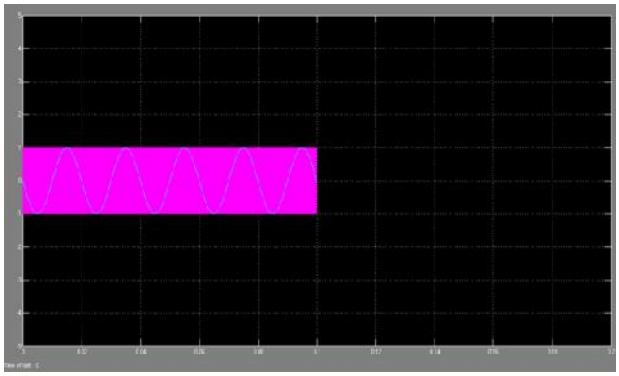

Fig. Simulation waveform for reactive power generation

In conclusion, the conduction and switching losses in the power devices of the proposed topology are quite similar to those of the H5 circuit. The main drawback is that larger capacitors are needed to reduce the ESR losses in the capacitor and ensure their life time. This issue can be alleviated by adding a thin film capacitor in parallel to the aluminum electrolyte one to absorb the high-frequency pulsating current. Fortunately, the clear advantage of the proposed topology is that it has better performance in eliminating the CM current.

VI. CONCLUSION

The concept of the virtual dc bus is proposed to solve the CM current problem for the transformerless grid-connected PV inverter. By connecting the negative pole of the dc bus directly to the grid neutral line, the voltage on the stray PV capacitor is clamped to zero. This eliminates the CM current completely. Meanwhile, a virtual dc bus is created to provide the negative voltage level. The required dc voltage is only half of the half-bridge solution, while the performance in eliminating the CM current is better than the full-bridge-based inverters. Based on this idea, a novel inverter topology is proposed with the virtual dc bus concept by adopting the switched capacitor technology. It consists of only five power switches and a single filter inductor. The proposed topology is especially suitable for the small-power single-phase applications, where the output current is relatively small so that the extra current stress caused by the switched ca-pacitor does not cause serious reliability problem for the power devices and capacitors. With excellent performance in eliminat-ing the CM current, the virtual dc bus concept provides a promis-ing solution for the transformerless grid-connected PV inverters.

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