An Efficient Implementation of Fully Functional DDR SDRAM Memory Controller Using HDL

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ABSTRACT: This paper presents a multichannel DDR SDRAM memory controller to be used as an IP in a set-top box compliant. A set-top box is comprised by modules that access an external memory sharing the same bus. A Dedicated Memory Controller is of prime importance in applications that do not contain microprocessors (high-end applications). The Memory Controller provides command signals for memory refresh, read and write operation and initialization of SDRAM. Our work will focus on ASIC Design methodology of Double Data Rate (DDR) SDRAM Controller that is located between the DDR SDRAM and Bus Master. The Controller simplifies the SDRAM command interface to standard system read/write interface and also optimizes the access time of read/write cycle. Double Data Rate (DDR) SDRAM Controller is implemented using Cadence RTL Compiler.

KEY WORDS: DDR SDRAM Controller, Read/Write Data path, RTL Compiler, HDL.

I. INTRODUCTION

Double data rate synchronous dynamic random-access memory (DDR SDRAM) is a class of memory integrated circuits used in computers.

Nowadays, Memory devices are almost found in all systems, high speed and high performance memories are in great demand. For better throughput and speed, the controllers are to be designed with clock frequency in the range of megahertz. As the clock speed of the controller is increasing, the design challenges are also becoming complex. Therefore the next generation memory devices require very high speed controllers like double data rate and quad data rate memory controllers. In this paper, the double data rate SDRAM Controller is implemented using ASIC methodology. Synchronous DRAM (SDRAM) is preferred in embedded system memory design because of its speed and pipelining capability. In high-end applications, like microprocessors there will be specific built in peripherals to provide the interface to the SDRAM. But for other applications, the system designer must design a specific memory controller to provide command signals for memory refresh, read and write operation and initialization of SDRAM. In this paper, the SDRAM controller, located between the SDRAM and the bus master, minimizes the effort to deal with the SDRAM memory by providing a simple system to interact with the bus master. Figure 1 is the block diagram of the DDR SDRAM Memory Controller that is connected between the bus master and SDRAM [1].

SDRAM's are classified based on their data transfer rates. In Single data rate SDRAM, the data is transferred on every rising edge of the clock whereas in double data rate (DDR) SDRAM's the data is transferred on every rising edge and every falling edge of the clock and as a result the throughput is increased. DDR SDRAM Controllers are faster and efficient than its counterparts. They allow data transfer at a faster rate without much increase in clock frequency and bus width.

Dynamic Random Access Memory

Dynamic Random Access Memory has memory cells with a paired transistor and capacitor requiring constant refreshing. DRAM works by sending a charge through the appropriate column (CAS) to activate the transistor at each bit in the column. When writing the row lines contain the state the capacitor should take on. When reading the sense amplifier determines the level of charge in the capacitor. If itis more than 50 percent, it reads it as a 1 otherwise it reads it as a 0.

II.IMPLEMENTATION OF BLOCK DIAGRAM

The DDR SDRAM Controller architecture is implemented using Verilog HDL. The methodology followed is ASIC design flow. The basic steps that an ASIC design must go through are Design entry and Analysis, Technology Optimization and Floor planning, Design Verification. The RTL Synthesis and Simulations are performed using existing tools like RTL Compiler.

Figure 1 shows the different blocks in top level reference design. The user interface module contains the I/O registers to latch system signals coming into the FPGA. The DDR controller module contains the DDR SDRAM controller, including I / Os to interface with the DDR SDRAM.

DDR SDRAM CONTROLLER ARCHITECTURE

DDR SDRAM Controller module receives addresses and control signals from the BUS Master. The Controller generates command signals and based on these signals the data is either read or written to a particular memory location. The DDR SDRAM Controller architecture is shown in Figure 2.

It consists of three modules:

1) Main control module
2) Signal generation module
3) Data path module.

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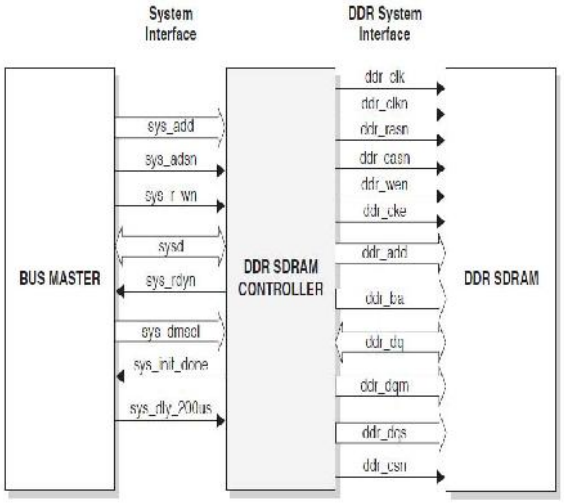

Fig. 1. DDR SDRAM controller system

The main control module has two state machines and a refresh counter. The two state machines are for initialization of the SDRAM and for generating the commands to the SDRAM. They generate iState and cState outputs according to the system interface control signals. The signal generation module now generates the address and command signals depending upon the iState and cState. The data path module performs the read and write operations between the bus master and DDR. Following are some of the important features of DDR SDRAM

Controller:

i. The DDR SDRAM Read and Write operations are simplified by the controller.

ii. For initializing the DDR SDRAM controller, separate state machines are designed internally.

iii. The access time for read and the write cycle is optimized based on the CAS latency and burst length of the DDR SDRAM.

iv. The auto refresh for the DDR SDRAM is done by the controller.

The main control module consists of three sub modules:

1) Initialization FSM module (INIT_FSM).
2) Command FSM module (CMD_FSM)
3) Counter module.

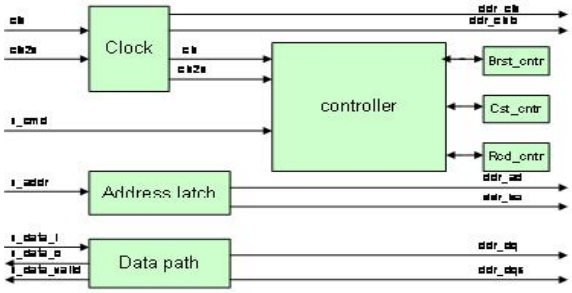

Figure 2: DDR Controller Architecture

III.DIFFERENT FUNCTIONAL BLOCKS

Address Latch

The basic function of address latch module is to gets its control signals from the controller and generates row, column and bank addresses for the DDR SDRAM. The address latch also generates different control signals like burst_max, cas_lat_max for the burst counter and cas latency counter.

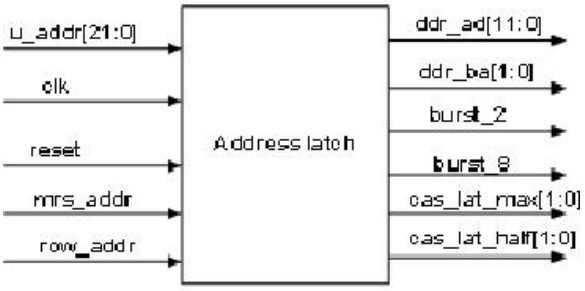

Figure 3: Address Latch Module

Data Path

One of the most difficult aspects of DDR SDRAM controller design is to transmit and capture data at double data rate. This module transmits data to the memories. The basic function of data path module is storing the write data and calculates the value for read data path.

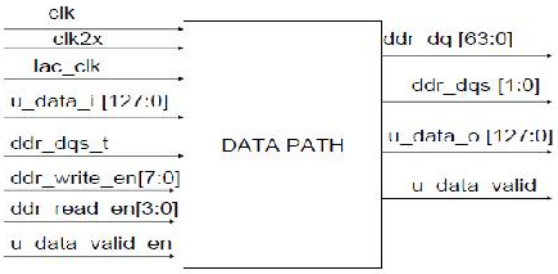

Figure 4: Data Path Module

Controller

The controller consists of a state machine which performs DDR SDRAM read and write accesses based on user interface request. The controller consists of a high performance timing & control state machine that observes all timing requirements and issues the commands to the memory devices at the shorted time possible. The pin diagram of controller is shown in figure 5:

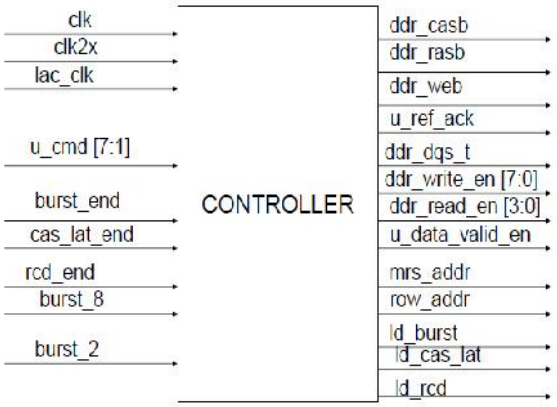

Figure 5: Controller Module

The DDR controller consists of a high performance memory controller for system requiring access to external devices with lowest latency and highest throughput. The controller accepts and decodes user interface commands and generates read, write, refresh commands. It also generates signals for other modules. The memory is initialized and powered up using a

defined process. The controller state machine handles the initialization process upon power up.
Controller state machine diagram

Initially the controller is in the IDLE state. That means no operation is performing. A PRECHARGE ALL command is then applied. This command is used to deactivate any open row in a bank or the open bank row in all banks. Once a bank is pre charged, it is in idle state and must be activated prior to any READ and WRITE operation. Next a LOAD MODE REGISTER command should be issued for the extended mode register to enable the DLL, then another LOAD MODE REGISTER command to the mode register to reset the DLL and to program the operating parameters. Again a PRECHARGE command should be applied which place the device in all banks in IDLE state. In the IDLE state two AUTO REFRESH cycles must be performed.
The controller next state could be PRECHARGE, LOAD_MR, REFRESH or ACT, depending upon the required command. The ACT command is used to open a row in a bank before starting any read or write operation. The controller state machine diagram is shown in figure 6.

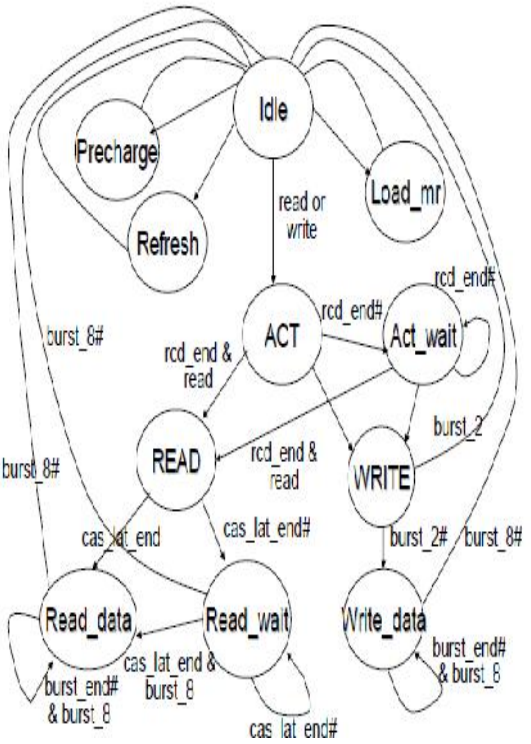

Figure 6:controller state machine diagram
Counter
The task of Burst Count is to count when there are consecutive READ and WRITE operations. While doing consecutive READ and WRITE operations, the Burst_count value determines when the next READ and WRITE command should be issued.
RESULTS
Figure 7 shows the RTL schematic of designed DDR SDRAM controller.

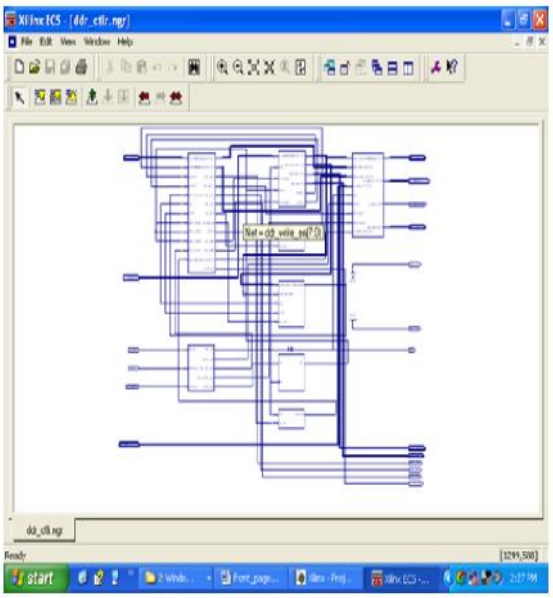

Figure 7: RTL schematic of DDR Controller

The following figures are the simulation result of controller, controller Write cycle and controller Read cycle obtained by using Modelsim 6.4b.

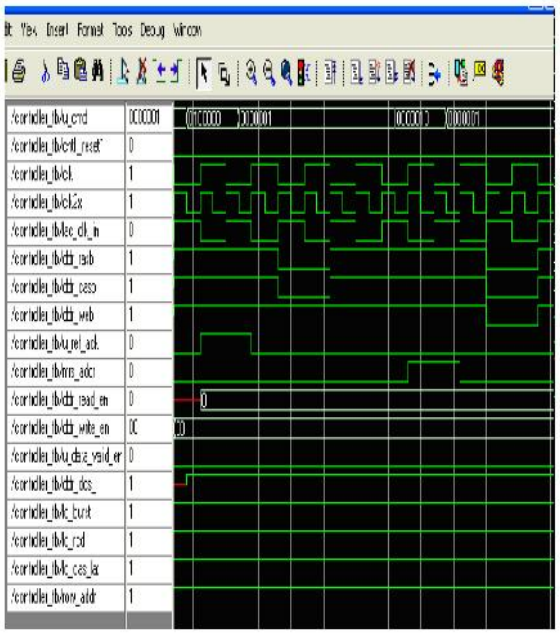

Figure 8: Simulation waveform for Controller

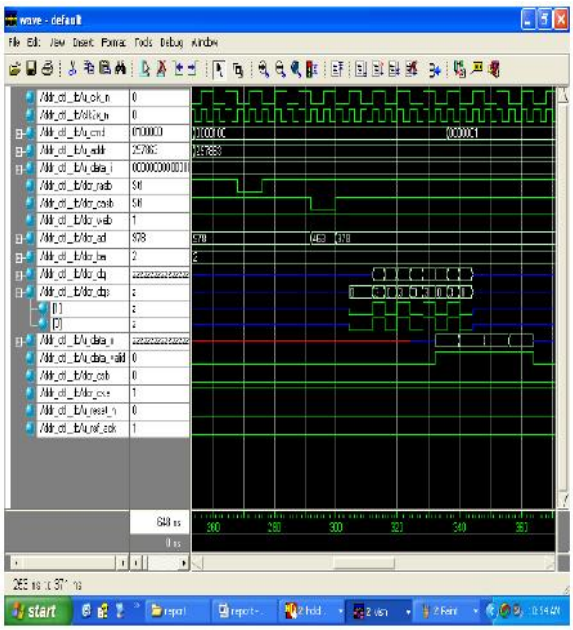

Figure 9: Simulation waveform for Controller Read Cycle

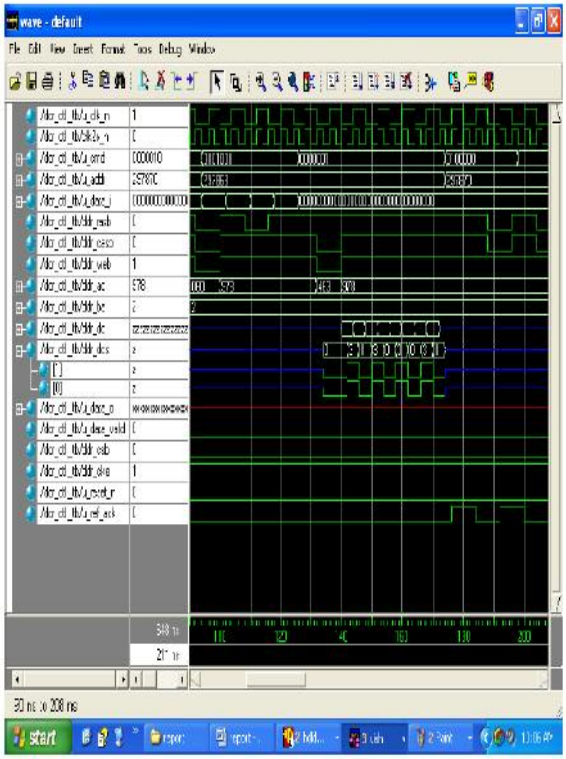

Figure 9: Simulation waveform for Controller Write Cycle

CONCLUSION

In this paper an efficient fully functional DDR SDRAM controller is designed. The controller generates different types of timing and control signals, which synchronises the timing and control the flow of operation. The memory system operates at double the frequency of processor, without affecting the performance. Thus we can reduce the data bus size. The drawback of this controller is complex schematic with large number of buffers in the circuit increases the amount of delay.

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