A Low Voltage CMOS Op-Amp

G.Laksmi Bhavani and A.Kalpana

Abstract: **A method is presented in this paper for the design of a high frequency CMOS operational amplifier (Op-Amp) which operates at 3V power supply using tsmc 0.18 micron CMOS technology. The OPAMP designed is a two-stage CMOS OPAMP followed by an output buffer. This Operational Transconductance Amplifier (OTA) employs a Miller capacitor and is compensated with a current buffer compensation technique. The unique behaviour of the MOS transistors in saturation region not only allows a designer to work at a low voltage, but also at a high frequency. Designing of two-stage op-amps is a multi-dimensional-optimization problem where optimization of one or more parameters may easily result into degradation of others. The OPAMP is designed to exhibit a unity gain frequency of 2.02GHz, the proposed compensation method results in a higher unity gain frequency under the same load condition. Design has been carried out in Tanner tools. Simulation results are verified using S-edit and W-edit.**

Keywords: CMOS Analog Circuit, Operational amplifier, Current Buffer Compensation

I. INTRODUCTION

Operational amplifiers (usually referred to as OPAMPs) are key elements in analog processing systems. OPAMP can be said to be the main bottleneck in an analog circuit. Ideally they perform the function of a voltage controlled current source, with an infinite voltage gain. Operational amplifiers are an integral part of many analog and mixed-signal systems. OPAMPs with vastly different levels of complexity are used to comprehend functions ranging from dc bias generation to high-speed amplification or filtering. The design of OPAMPs continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies [4]. Designing high-performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages. At large supply voltages, there is a tradeoff among speed, power, and gain, amid other performance parameters. Often these parameters present contradictory choices for the op-amp architecture. Speed and accuracy are two most important properties of analog circuits, however optimizing circuits for both aspects leads to contradictory demands. The realization of a CMOS OPAMP that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem. The simulation results have been obtained by tsmc 0.18 micron CMOS technology. Design has been carried out in Tanner tool. Simulation results are verified using S-edit and W-edit.

II. THE VARIOUS STAGES INCORPORATED IN THE DESIGN

In the past few years, various new-fangled topologies have evolved and have been employed in various applications. Here we have chosen a simple differential pair amplifier (high noise immune) for input amplifier, common source amplifier (high gain) for output amplifier, a current mirror circuit (free from voltage sources; utilizing single current reference source) as a biasing circuit, and a current buffer compensation circuit in conjunction with a Miller capacitance in series with one another.

The topology of the circuit designed is that of a standard CMOS op-amp. It comprised of three subsections of circuits, namely differential gain stage, second gain stage and bias strings. Examining the subsections further will provide valuable insight into the operation of this Amplifier.

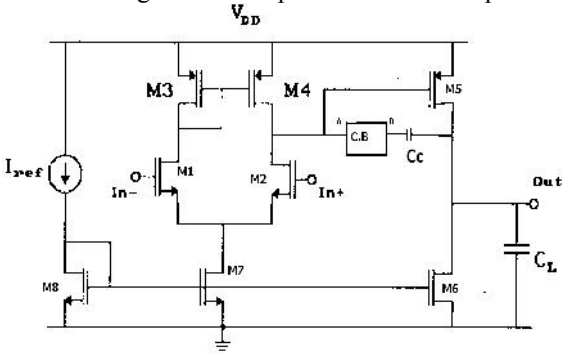

Figure 1: Two stage OPAMP with the compensation block

The first subsection of interest is the differential gain stage which is comprised of transistors M1 to M4. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The transconductance of this stage is simply the transconductance of M1 or M2. M3 and M4 are the active load transistors of the differential amplifier. The current mirror active load used in this circuit has three distinct advantages. The current mirror topology performs the differential to single-ended conversion of the input signal, and finally, the load also helps with common mode rejection ratio. The biasing of the operational amplifier is achieved with only three transistors along with a current source. Transistor M8 and the current source supply a voltage between the gate and source of M7 and M6. Transistors M6 and M7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. M8 is diode connected to ensure it operate in the saturation region. Proper biasing of the other transistors in the circuit (M1 – M5) is controlled by the node voltages present in the circuit itself. Most importantly, M5 is biased by the gate to source voltage (VGS) set up by the VGS of the current mirror load as are the transistors M1 and M2.

III.THE DESIGN APPROACH

This work presents a design that illuminates the speed and gain recompense of two a two-stage OPAMP along with high unity gain frequency. This work deals with ingenious design criterion for two-stage CMOS transconductance operational

amplifiers. A novel and simple design procedure is presented, which allows electrical parameters to be univocally related to the value of each circuit element and biasing value. This design yields an accurate performance optimization eliminating unnecessary circuit constraints. Bandwidth optimization strategies are also discussed. SPICE simulations based on the proposed procedures are given which closelyconsent the expected results.

At the very onset of the design, the differential amplifier bias current (Iss) is selected considering the gain, CMRR, power dissipation, noise, unity gain frequency and slew rate matching considerations. The small signal gain of the differential amplifier is given by

$$A_1 = g_{m1}(r_{o1} \| r_{o2})$$

After compensation of the right half plane zero, the maximum achievable gain -bandwidth product is limited by the phase margin, Ø, we must properly set the ratio of the second pole, Wp2 to the gain bandwidth product, WGBW which is equal to the tangent K of the phase margin.

$$K = \tan(\emptyset) = \frac{W_{p2}}{W_{GBW}}$$

Again, it is also seen that WGBW depends on the transconductance of the first stage, gmI and on the compensation capacitance CC and is related by the equation

$$W_{GBW} = \frac{g_{m1}}{C_c}$$

During the linear settling period the output voltage settles to its final value in a small-signal linear fashion. In this work, the model of the settling time developed by Turchetti [20] has been used because of its simplicity.

As per this model,

Tset = Ts1+Ts2

IV.RESULTS

In order to corroborate the proposed compensation strategy, the two-stage OPAMP in the figure was designed using the model parameter of tsmc0.18 micron CMOS process. The design parameters along with the electrical parameters yielded are as given in the table1. This circuit operates efficiently in a closed loop feedback system, while high bandwidth makes it suitable for high speed applications. The circuit operating conditions includes the room temperature as the operating temperature with a power supply of 3V and a load of 10fF.

For the frequency response plot, an ac signal of 1V is swept with 5 points per decade from a frequency of 10KHz to 4GHz. Fig.5 illustrates the frequency response which shows a dc gain in dB versus frequency in Hz(in log scale) and phase margin of OPAMP in open loop. The dc gain is found to be 49.02dB and phase margin 60.50 which is good enough for an OPAMP operating at a high frequency. A unity gain frequency of 2.02GHz is excellent for an OPAMP when all the other parameters are also set at an optimised value.

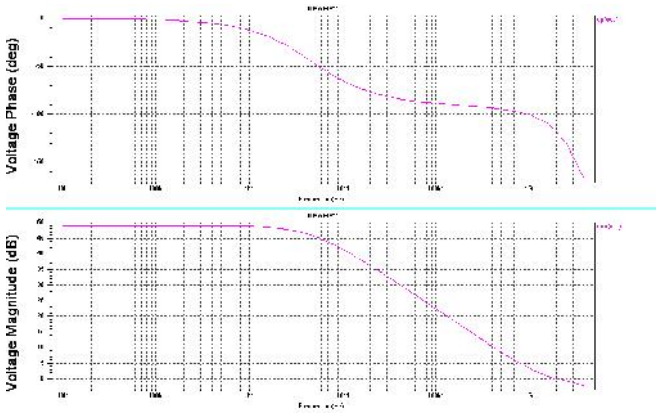

Figure 2: Frequency response of the OPAMP

PSRR measures the influence of power supply ripple on the OPAMP output voltage. It is the ratio of voltage gain from the input to output (open loop) to that from the supply to the output. PSRR can be calculated by putting the OPAMP in the unity gain configuration with the input shorted. The Miller compensation capacitance allows the power supply ripple at the output

to be large enough.

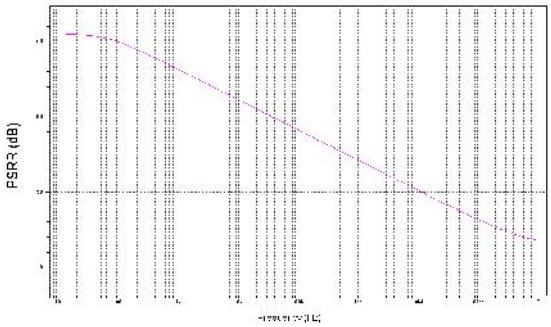

Figure 3: PSRR of the OPAMP

The design parameters		The electrical parameters yielded	
M1	15/0.2 µm/ µm	g_{mI}, g_{mII}	806µ, 537µ
M2	15/0.2 µm/ µm	Phase margin, Ø	60.5^0
M3	3.2/0.4µm/ µm	C_{01}	24.8fF
M4	3.2/0.4µm/ µm	Unity gain frequency, f_T	2.02GHz
M5	6.2/0.2µm/ µm	DC Gain	49.02dB
M6	1.2/0.2µm/ µm	PSRR(+ve)	154dB
M7	0.8/0.2µm/ µm	Settling time	0.5nsec
M8	0.4/0.2µm/ µm	Slew rate (+ve,-ve)	1.41V/µs; 1.42V/µs
Mb	3.2/0.2µm/ µm	Common mode gain	0.54957dB
I_{ref}	50µA	CMRR	39dB|
Vdd	3V	Noise	1.64µV/sqrt(Hz)
C_L	10fF	Power consumption	39.6µW

Table 1: The dimensions incorporated and the electrical parameters

V. CONCLUSIONS

Here, the gain has been increased by employing thin and long transistors into the design at output stage and wide transistors in input stage. These two techniques are able to increase the gain up to a great extent by increasing the output resistance and input transconductance respectively. Here the improvement in unity gain bandwidth has been done by increasing the bias current which decreases the DC gain and increases power dissipation little bit, still provides a good alternative control for an operational amplifier to operate at a high frequency. Introduction of each stage in multi-stage OPAMPs exhibits an additional pole into the system which can create problems in stability. A simple looking OPAMP

design problem becomes a harder one when it comes to optimizing all the parameters at a time. A careful analysis of circuit and deep insight into the circuit topologies and device operations leads to good implementation and desired results.

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