

An Efficient High Speed Wallace Tree Multiplier

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Abstract: The Wallace tree multiplier is considered as faster than a simple array multiplier and is an efficient implementation of a digital circuit which is multiplies two integers. A Wallace tree multiplier is a parallel multiplier which uses the carry save addition algorithm to reduce the latency. There are many researchers have been worked on the design of increasingly more efficient multipliers. They aim at achieve higher speed and lower power consumption even while occupying reduced silicon area. The Wallace tree basically multiplies two unsigned integers. The new architecture enhances the speed performance of the widely acknowledged WTM.

I.Introduction:

A multiplier can be divided into further three stages: - Partial products generation (PPG) stage is the first stage in which the multiplicand and the multiplier are multiplied bit by bit to generate the partial products. Partial products addition stage or reduction of partial products (PPR) is the second stage which is the most important as it is the most complicated and that determines the speed of the overall multiplier and the final addition stage or carry-propagate addition (CPA) using different compressors have been widely employed in the high speed multipliers to lower the latency of the partial product accumulation stage . In order to employ the processor for digital signal processing applications, a modified Wallace tree multiplier which uses compressors circuits to obtain low power and high speed operation in the Arithmetic Logic Unit (ALU) . In digital CMOS design, the well-known power-delay product is commonly used to evaluate the value the merits of designs.

PARTIAL PRODUCT USING COMPRESSOR

The multiplier architecture comprises of a partial product generation stage, partial product reduction stage and the final addition stage. In the proposed architecture, multi bit compressors are used for realizing the reduction in the number of partial product addition stages.

The combined factors of low power, low transistor count and minimum delay makes the 3:2,4:2 and 5:2 compressors, the appropriate choice. In these compressors, the outputs generated at each stage are efficiently used by replacing the XOR blocks with multiplexer blocks .The select bits to the multiplexers are available much ahead of the inputs so that the critical path delay is minimized.

The multiplier architecture proposed comprises of a partial product generation stage (PPG), partial product reduction stage (PPR) and the final addition stage or carry-propagate addition (CPA). In the partial products reduction stage the latency of the Wallace tree multiplier can be reduced by decreasing the number of adders. Realization and reduction in the number of partial product addition stages are using multi-bit compressors.

3:2 Compressor

The 3:2 Compressor is a combinational circuit which sum up three binary inputs of one bit and returns sum and carry of one bit.

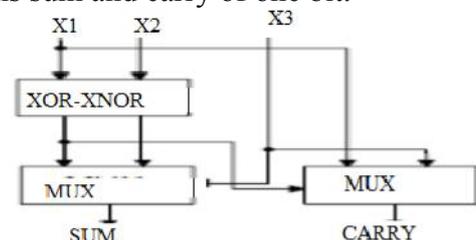


Figure 1: A 3:2 Compressor by using universal gates

It is used as a full adder. Figure1 shows block diagram of the 3:2 compressor, it has three inputs

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X_1, X_2 and X_3 and two outputs sum and carry.

The equations governing the outputs of the 3:2 compressor architecture is shown below.

$$\text{Sum} = X_1 \oplus X_2 \oplus X_3$$

$$\text{Carry} = X_1 X_2 + X_2 X_3 + X_3 X_1$$

Table.1 has three 1-bit inputs name as X_1, X_2 and X_3 and two outputs sum and carry. For example a binary input of “001” results in an output of $0 + 0 + 1 = 10$. Here 1he sum represents bit one, $\text{Sum} = „1”$ while the carry-out represents carry = „0” of the results.

4.2.2 4:2 Compressor

The 4:2 compressors has 4 inputs X_1, X_2, X_3 and X_4 and 2 outputs Sum and Carry along with a Carry-in (C_{in}) and a Carry-out (C_{out}).

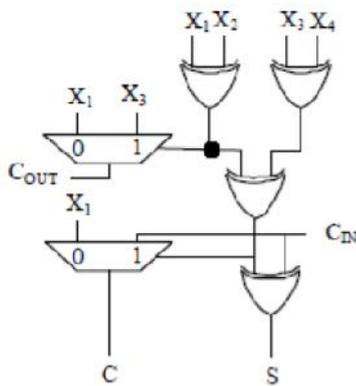


Figure 2 :A 4:2 Compressor (DPL logic)

The block diagram of 4:2 compressor is composed of two serially connected 3:2 Compressors as shown in figure 2 (a) and (b). First 3:2 compressor has three inputs x_1, x_2 and x_3 , the sum and carry outputs of this compressor are s_1 and Carry1. Second 3:2 compressor has inputs S_1, X_4 and „0” as third input, produces Sum and Carry2.

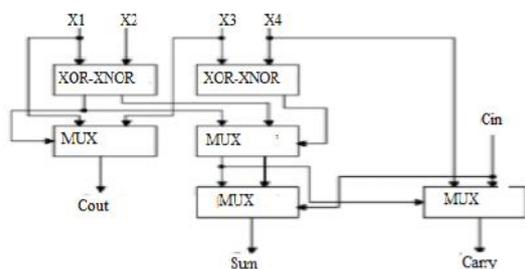


Figure 3 : A 4:2 Compressor with universal gates.

Double pass transistor logic (DPL) implementation of the gate logic structure shown above has been shown to exhibit lower power consumption and higher speed performance compared to earlier designs due to its reduction of the internal load capacitances in the critical path.

The use of transmission gate multiplexer in the construction of compressors further reduces the number of transistors to 8 which would have been 12 in the case of conventional CMOS multiplexer. On the other hand, the use of a 4:2 compressor reduces the latency to 3. Hence, two full adders can be replaced by a single 4:2 compressor. The equations governing the outputs of the 4:2 compressor architecture is shown below.

4.2.3 5:2 Compressor

The 5:2 Compressor is a combinational circuit which sum up five binary inputs of one bit and returns sum and carry of one bit.

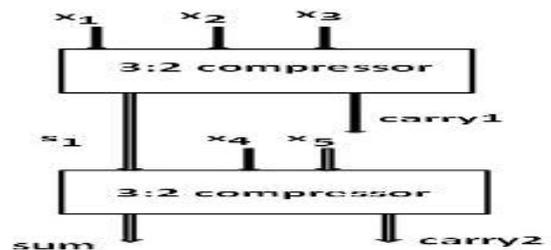


Figure 4 : Block diagram of 5:2 compressor using two 3:2 compressors

MULTIPLICATION LOGIC

Considering an example of 8 bit multiplication in which 8 bit input is $X_7X_6X_5X_4X_3X_2X_1X_0$ and multiplier is $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$. The multiplication process is shown in figure 4(a). There is the requirement of 64 AND logics. First Y_0 is multiplied with $X_7X_6X_5X_4X_3X_2X_1X_0$ and results $X_0Y_0, X_1Y_0, X_2Y_0, X_3Y_0, X_4Y_0, X_5Y_0, X_6Y_0$ and X_7Y_0 . After it Y_1 is multiplied with $X_7X_6X_5X_4X_3X_2X_1X_0$ and results $X_0Y_1, X_1Y_1, X_2Y_1, X_3Y_1, X_4Y_1, X_5Y_1, X_6Y_1$ and X_7Y_1 . Similarly all multiplications are taken place. In each step there is one binary shift in the resultant logic. All AND logics are represented by one bit representation starting from K_0 to K_{63} sequentially as shown in figure 4(b). After completion of 64 AND logic there is an additive process which is shown in figure 4(c). The addition can be done using a tree formed

itself. This is done using 3:2 compressor, 4:2 compressor and 5:2 compressor which are the optimized solutions instead of using 3:2 compressors only. This addition is possible using 3:2 compressors only but the implementation using 4:2 and 5:2 reduces the latency and increases the speed. The addition is shown using Wallace tree shown in figure . In the process the sum output of intermediate compressors is the input for next compressors in the same column and the generated carry for the corresponding adders are propagated to next column adders. The result will be of 16 bits represented by $[P_{15} \dots P_0]$.

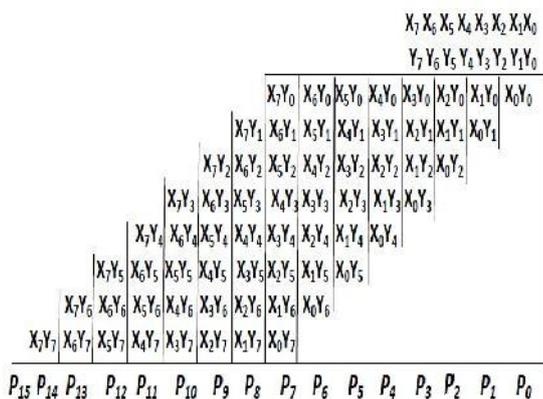


Figure 5 . Multiplier (8 bits)

common counter used is the 3:2 counter which is a Full Adder.. The final results are added using usually carry propagate adder. The advantage of Wallace tree is speed because the addition of partial products is now $O(\log N)$. A block diagram of 4 bit Wallace Tree multiplier is shown in below. As seen from the block diagram partial products are added in Wallace tree block. The result of these additions is the final product bits and sum and carry bits which are added in the final fast adder (CRA).

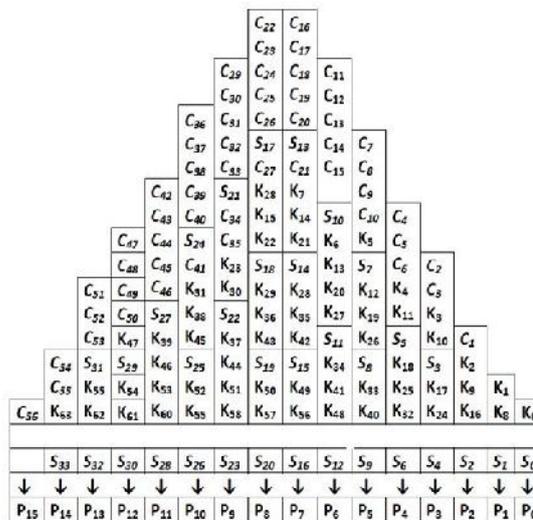


Figure 7: Wallace Tree Multiplier using optimized Compressor

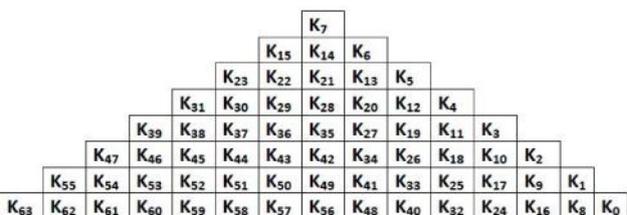


Figure 6. Multiplication wallace Logic tree

Several popular and well-known schemes, with the objective of improving the speed of the parallel multiplier, have been developed in past. Wallace introduced a very important iterative realization of parallel multiplier. This advantage becomes more pronounced for multipliers of bigger than 16 bits. In Wallace tree architecture, all the bits of all of the partial products in each column are added together by a set of counters in parallel without propagating any carries. Another set of counters then reduces this new matrix and so on, until a two-row matrix is generated. The most

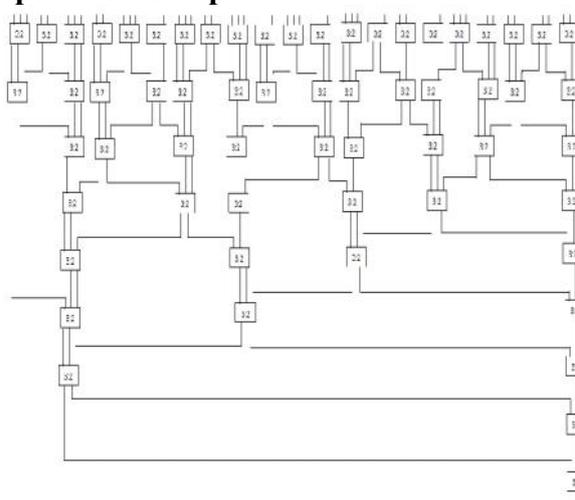


Figure 8 : Wallace Tree using 3:2 compressors

The 3:2 compressors make use of a carry save adder .The carry save adder outputs two numbers of the same dimensions as the inputs, one is a sequence of partial sum bits and other is a sequence of carry bits. In carry save adder, the

carry digit is taken from the right and passed to the left, just as in conventional addition; but the carry digit passed to the left is the result of the previous calculation and not the current one.

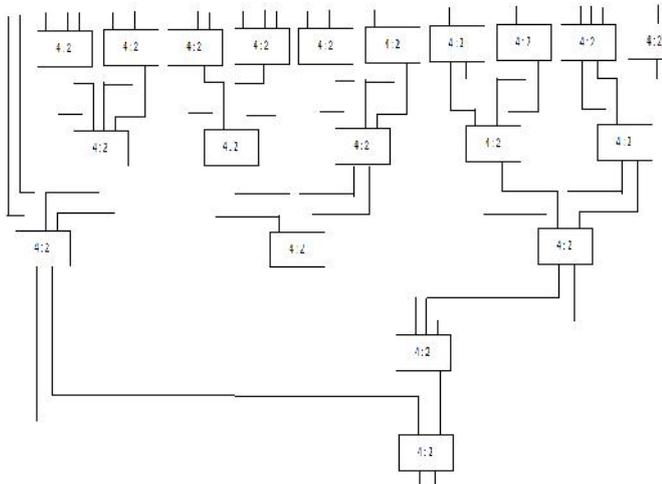


Figure. 22: Wallace Tree using 4:2 compressors

So in each clock cycle, carries only have to move one step along and the clock can tick much faster. Also the carry-save adder produces all of its output values in parallel, and thus has the same delay as a single full-adder. The 4:2 compressors have been widely employed in the high speed multipliers to lower the latency of the partial product accumulation stage. A 4:2 compressor can be built using two 3:2 compressors. Owing to its regular interconnection, the 4:2 compressor is ideal for the construction of regularly structured Wallace Tree with low complexity.

In this section performance measures of multipliers discussed so far are summarized and compared. These results were obtained after synthesizing individual architectures targeting Xilinx FPGA 4052XL-1HQ240C. All comparisons are based on the synthesis reports keeping one common base for comparison. We summarize Area (Total number of CLBs required), Delay and Power Consumption and also calculate Delay·Power (DP), Area·Power (AP), Area·Speed (AT) and Area·Speed² (AT²) product.

From the Table we can see that delay of Wallace tree multiplier and Combined Booth-Wallace tree multiplier is almost the same and is the least. Hence they are fastest among five multipliers. DP product is also the least for the above two multiplier and are a good choice for this

performance measure. Serial Parallel multiplier is a best choice when speed is not important but reduced area and power consumption is of more interest and also for AP and AT product Serial Parallel multiplier is a good choice. However, one of the most important performance parameter is AT². From the table we see that Modified Booth-dWallace Tree multiplier is the best choice as far as AT² is concerned. The Serial Parallel multiplier which is a good choice for AP and AT product has worst performance for AT².

IMPLEMENTATION RESULTS:

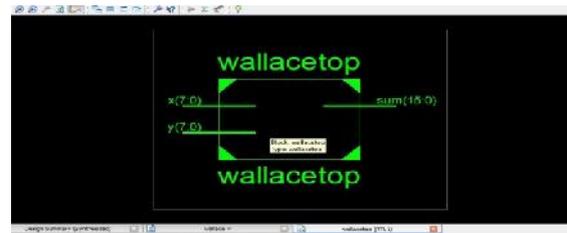


Figure 9. 8 bit multiplier

Device utilization summary is the report of used device hardware in the implementation of the chip such as RAM, ROM, slices, flip flops etc. Synthesis report shows the complete details of device utilization as total memory utilization. Timing details provides the information of net delay, minimum period, minimum input arrival time before clock and maximum output required time after clock. Selected Device is 3s250epq208-5. It is the FPGA device at which designed is targeted

CONCLUSTION

The simulation and synthesis of multiplier is done in Xilinx ISM 14.2 and functionally tested in Modelsim with different test cases. The implementation is followed using 3:2 compressor, 4:2 compressor, 5:2 compressors. The same implementation could be done using 3:2 compressors only but we optimized the multiplier design using 4:2 and 5:3 compressors also.

Due to which the combinational path delay is 14.263 ns and memory utilization is found 144492 kilobytes. In future we can enhance the performance of multiplier by the synthesis on Virtex-7 FPGA and implementation of „N“ bits multiplier.

The results prove that the proposed architecture is more efficient than the existing one in terms of delay. This approach may be well suited for multiplication of numbers with more than 16 bit size for high speed applications.

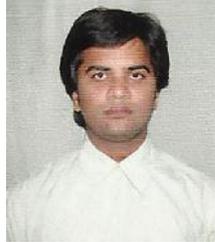
The power of the proposed multiplier can be explored to implement high performance multiplier in VLSI applications. Wallace tree multiplier using booth algorithm is very a good technique for high speed applications, its implementation with different logics in VLSI. Further the work can be extended for optimization of said multiplier to improve the power.

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