DESIGN AND IMPLEMENTATION OF THE ADVANCED MICROCONTROLLER BUS ARCHITECTUREAXI-APB BRIDGE ON FPGA

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ABSTRACT: ***ARM introduced the Advanced Microcontroller Bus Architecture (AMBA) 4.0 and its specifications define five buses/interfaces: Advanced eXtensible Interface (AXI), Advanced High-performance Bus (AHB), Advanced System Bus (ASB), Advanced Peripheral Bus (APB) and Advanced Trace Bus (ATB). AMBA bus is widely used in the high-performance SoC designs.***

In this paper we are using advanced extensible Interface bus (AXI) 4.0 and Advanced Peripheral Bus (APB) to build compatibility between two Integrated Circuits(IC's) which are used in System on Chip (SoC) designs. AMBA bus protocol has become the de facto standard SoC bus. That means more and more existing Integrated Circuits(IC's) must be able to communicate with AMBA 4.0 bus. Based on AMBA 4.0 bus, we are designing an Advanced extensible Interface (AXI)-Advanced Peripheral Bus (APB) Bridge, which translates the AXI4.0-lite transactions into APB 4.0 transactions. The bridge provides interfaces between the high-performance AXI bus and low-power APB domain. The AMBA specification defines an on-chip communication standard for designing high-performance embedded microcontrollers.

I. INTRODUCTION

The Advanced Microcontroller Bus Architecture (AMBA) is used as the on-chip bus in system-on-a-chip (SoC) designs. Since its inception, the scope of AMBA has gone far beyond microcontroller devices, and is now widely used on a range of ASIC and SoC parts including applications processors used in modern portable mobile devices like smartphones. The AMBA protocol is an open standard, on-chip interconnect specification for the connection and management of functional blocks in a System-on-Chip (SoC). It facilitates right-first-time development of multi-processor designs with large numbers of controllers and peripherals.There are many companies that develop core IP for SoC products. The interfaces to these cores can differ from company to company and can sometimes be proprietary in nature. The SoC developer then must expend time, effort, and money to create "bridge" or "glue" logic that allows all of the cores inside the SoC to communicate properly with each other. Incompatible interfaces are thus barriers to both IP developers and SoC developers. SoC integrated circuits envisioned by this subcommittee span a wide breadth of applications, target system costs, and levels of performance and integration.

Integrated circuits have entered the era of System-on-a-Chip (SoC), which refers to integrating all components of a computer or other electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions – all on a single chip substrate. With the increasing design size, IP is an inevitable choice for SoC design. And the widespread use of all kinds of IPs has changed the nature of the design flow, making On-Chip Buses (OCB) essential to the design.

Of all OCBs existing in the market, the AMBA bus system is widely used as the de facto standard SoC bus. On March 8, 2010, ARM announced availability of the AMBA 4.0 specifications. As the de facto standard SoC bus, AMBA bus is widely used in the high-performance SoC designs. The AMBA specification defines an on-chip communication standard for designing high-performance embedded microcontrollers.

ARM introduced the Advanced Microcontroller Bus Architecture (AMBA) 4.0 specifications in March 2010, which includes Advanced extensible Interface (AXI) 4.0. AMBA bus protocol has become the de facto standard SoC bus. That means more and more existing IPs must be able to communicate with AMBA 4.0 bus. Based on AMBA 4.0 bus, this design is an Intellectual Property (IP) core of AXI (Advanced extensible Interface) Lite to APB (Advanced Peripheral Bus) Bridge, which translates the AXI4.0-lite transactions into APB 4.0 transactions. The bridge provides interfaces between the high-performance AXI bus and low-power APB domain.The aim of this paper is to design an interface between APB and UART which is used to connect external peripherals. The APB interface allows access to the UART through APB. UART is being used in SoC which consists of transmitter, receiver and baud rate generator and therefore connecting it to the APB which is a peripheral bus in AMBA to connect different peripherals, hence APB interface design with UART is needed.

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SoCbus.That means more and more existing IPs must be able to communicate with AMBA 4.0 bus. Based on AMBA 4.0 bus, we designed an Intellectual Property (IP) core of AXI4LITE-APB Advanced Peripheral Bus (APB) Bridge, which translates the AXI4.0-lite transactions into APB 4.0 transactions.There will be data missing when high performance modules like DMA, RAM, and Processor are directly interfaced to low performance modules/devices like peripheral devices. By this the system will slowdown in data transfer and there will be no synchronization of clock timings between the modules. To overcome this problem a bridge should be provided which makes good data communication and good synchronization of timings between modules at any frequency. The data transfers are done like two-way control operation that is source is master, destination is slave and vice versa. The bridge provides high speed of data transactions between high performance modules and low performance Devices. The Bridge provides interfaces between the high-performance AXI bus and low-power APB domain.

In previous microcontrollers, there is no on chip bus which increases external connections which leads to increase in complexity, reduces speed and consumes more power. The APB interface allows access to the UART through APB. UART is being used in SoC which consists of transmitter, receiver and baud rate generator and therefore connecting it to the APB which is a peripheral bus in AMBA to connect different peripherals, hence APB interface design with UART is needed.Software Used: Xilinx ISE 9.2 has been used for Simulation, Synthesis andImplementation.Hardware used: Xilinx Spartan (Family), 3S500E (Device), FG320 (Package), -4(Speed Grade) FPGA device.

II. DESIGN AND IMPLEMENTATION OF AXI-APB INTERFACING UART

A.Proposed Architecture

The UART-APB core is a serial communication controller with a serial data interface that is intended primarily for embedded systems and designing ASIC. The UART-APB core can be used to interface directly to industry standard UARTs. The UART-APB core is intentionally a subset of full UART capability to make the function cost-effective in a programmable device. In Several Control systems, UART a kind of serial communication circuit is used widely. A universal asynchronous receive/transmit (UART) is an integrated circuit which plays the most important role in serial communication.

The APB interface allows access to the UART through APB. UART is being used in SoC which consists of transmitter, receiver and baud rate generator and therefore connecting it to the APB which is a peripheral bus in AMBA to connect different peripherals, hence APB interface design with UART is needed.

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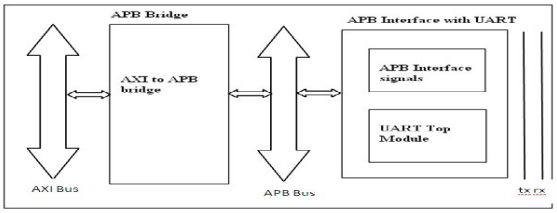

FIG .1:AXI- APB Proposed architecture

B.Design of UART:

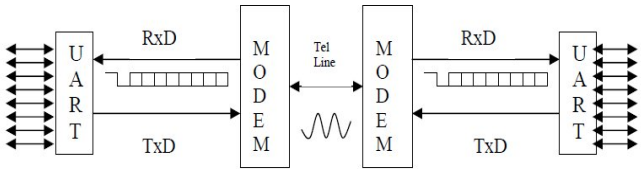

FIG 2: Block Diagram:

A universal asynchronous receiver/transmitter (usually abbreviated UART and pronounced) is a type of "asynchronous receiver/transmitter", a piece of computerhardware that translates data between parallel and serial forms.The Universal Asynchronous Receiver/Transmitter (UART) controller is the key component of the serial communications subsystem of a computer. The UART takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes.

When transmitting, the UART takes 8 bits of parallel data and converts the data to a serial bit stream that consists of a start bit (logic 0), 8 data bits (least significant bit first), and one or more stop bits (logic 1).The structure of UART is as shown in below figure, consists of Transmitter part and Receiver part, rather we can say consists of 3 units, transmitter circuit, receiver circuit and Control/Status Registers.

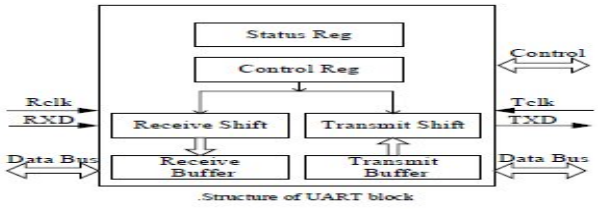

FIG 3: Structure of UART Block

C.Design of UART Transmitter

The Block diagram of UART Transmitter is as shown in below figure. The data is loaded from Data Bus into TBR (Transmit Buffer Register) and from TBR to TSR (Transmit Shift Register), based on the control and status signals produced by the Control unit. The Size of TSR is taken in such a way that, it should accommodate the START and STOP bits along with the Data bits which are loaded from the Data Bus.

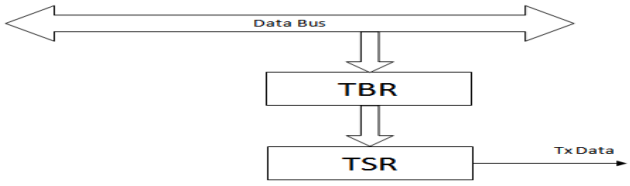

FIG4: UART Transmitter Unit

Correspondingly, the data in TSR will keeps updating with 0's; will be completely filled with 0's, after transmission of the complete data packet.

D.Design of UART Receiver

The Block diagram of UART Receiver is as shown in below figure. The data receiving will be captured using receiving baud clock and then loaded into RSR (Receive Shift Register) and from RSR to RBR (Receive Buffer Register), and then to Data Bus, based on the control and status signals produced by the Control unit. The Size of RSR is taken in such a way that, it should accommodate the START and STOP bits along with the Data bits which are loaded from the Data Bus.

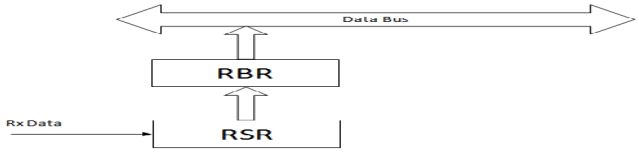

FIG 5: UART Receiver

E.Baud Rate Generator

The Baud Rate Generator is a programmable transmit and receive bit timing device. Given the programmed value, it generates a periodic pulse, which determines the baud rate of the UART transmission. This pulse is used by the receiver and transmitter circuit to generate a sampling pulse for sampling the received serial data and to determine the bit width of the transmit data

III. UART-APB Interface

The UART-APB core is a serial communication controller with a serial data interface that is intended primarily for embedded systems and designing ASIC. The UART-APB core can be used to interface directly to industry standard UARTs. The UART-APB core is intentionally a subset of full UART capability to make the function cost-effective in a programmable device. In Several Control systems, UART a kind of serial communication circuit is used widely. A universal asynchronous receive/transmit (UART) is an integrated circuit which plays the most important role in serial communication.

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UART APB Interface Block diagram

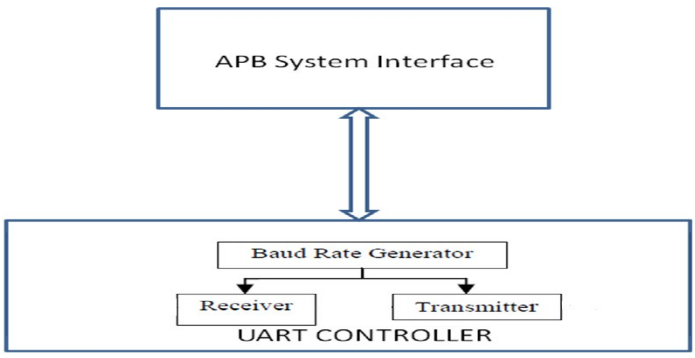

FIG 6: UART APB Interface Block diagram

IV. SIMULATION AND SYNTHESIS RESULTS

A.Simulation Results of APB Bridge: The APB UART interface has been designedconsisting of APB which is a

peripheral bus in AMBA used to connect different peripherals.

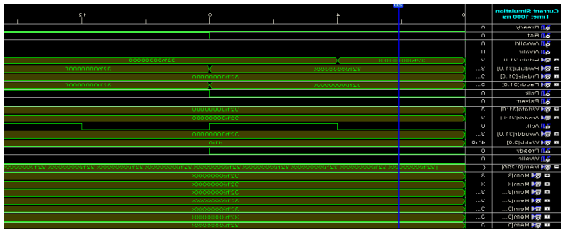

Fig 7:Simulation Results of APB Bridge

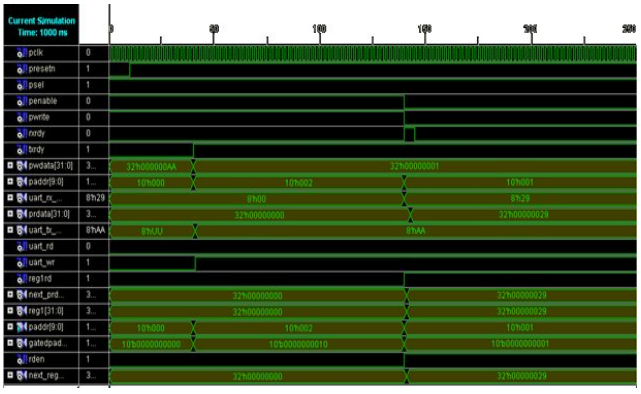

Fig 8:Simulation Results of APB Interface with UART

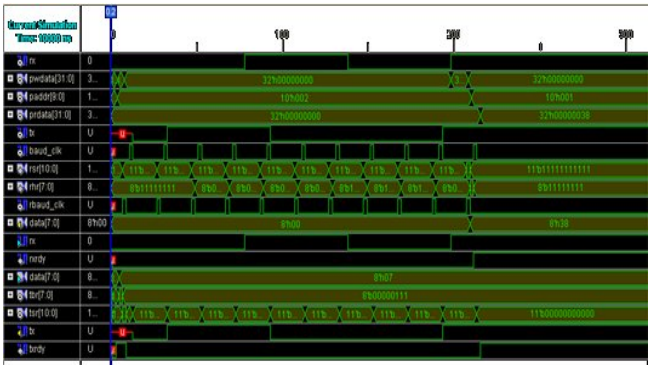

Fig 9:Simulation Results of Top module of APB Interface with UART

B.Synthesis report:

a.Device utilization summary

Selected Device: 3s500efg320-4

Number of Slices:		752 out of 4656 16%
Number of Slice Flip Flops:		780 out of 9312 8%
Number of 4 input LUTs:		2901 out of 9312 31%
Number used as logic:	1235	
Number used as RAMs:		1666
Number of IOs:	149	
Number of bonded IOBs:		121 out of 232 52%
IOB Flip Flops:	2	
Number of GCLKs:		2 out of 24 8%

B.Timing Summary

Speed Grade: -4

Minimum period: 8.418ns (Maximum Frequency: 118.793MHz)

Minimum input arrival time before clock: 6.251ns

Maximum output required time after clock: 5.115ns

Maximum combinational path delay: No path found

C. RTL Schematic

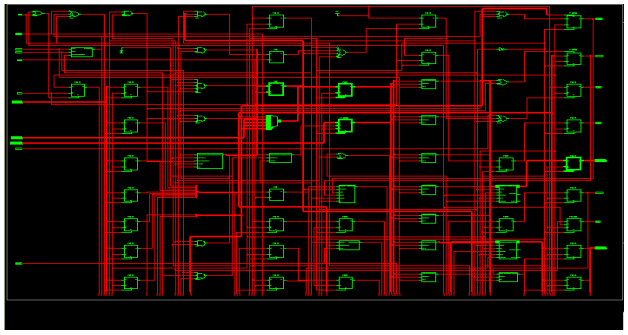

Fig 10: RTL Schematic

V. CONCLUSION AND FUTUTE SCOPE

AMBA 4.0 compatible APB UART controller is an on chip bus which can run at different clock rates and is a simpler, lower-speed, low-power bus.AMBA AXI4 Lite is a plug and play IP protocol released by ARM, defines both bus specification and a technology independent methodology for designing, implementing and testing customized high-integration embedded interfaces. The data and address are of 32 bits. The PCLK clock is completely independent of ACLK clock. It can support up to 16 APB peripherals.The data to be read or written to the slave is given by the master and is read or written to a particular address location of slave. In this work data transactions were carried out using AMBA AXI4 protocol modeled in Verilog hardware

description language (HDL) and simulation results have been successfully verified.

To increase the IP reuse ability is the key issue to accelerate the SoC integration. By adding a built-in ICE (integrated chip environmental) and make the SoC verification more quick and flexible.It is used for Easy to Configure,AMBA Compatible design to integrate in SOC (System-On-Chip),Low power consumption,Lowcomplexity,It supports 32bit and 66 MHz signal.theApplications of AMBA is used in Embedded processor applications,Mainly used in full duplex communication,It is used in Smartphones and It is used in industrial applications**.**

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