A Second Generation Current Mode Conveyor Based Analog Multiplier/Divider Along with Applications

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Abstract—the basic building block of second generation current controlled current conveyor based analog multiplier/divider is proposed. The proposed circuit uses two CCCII+ with no resistors, no capacitors, no MOS transistors and without using current controlled ground resistor (CCGR). With proper selection of the applied input currents, the proposed schematic can perform the function as a current follower, four quadrant multiplication and frequency doubling. 0.35µm specifications using PSPICE results are obtained and are included.

Index Terms—analog, current mode, CCCII+, CCGR, frequency doubling.

I. INTRODUCTION

Now a day, in analog signal processing circuits, current signals are more used for operating the circuits rather than voltage form. In current mode signal processing circuits, both input and output are taken in the form of current mode by dominating the voltage mode. Due to the interconnection of current mode signals, it provides higher bandwidth as compared to voltage mode circuits. From that the current signals can be transmitted fast over the link and hence it will increase the speed of operation.

In current mode design circuits by which current is used as the active variable in preference to voltage, either throughout the whole circuit or only in certain critical areas. A current mode design circuits has considerably more attention because of their advantages such as speed, better linearity, wider bandwidth, bigger dynamic range and lesser power dissipation compared with voltage mode counter-parts such as operational amplifiers.

In addition current mode functions exhibits simpler architectures and certain applications benefits from operating in the current mode domain. Speed is maximized by driving currents rather than voltages.

The current mode circuit techniques are classified such as current conveyors, operational transconductance amplifiers and switched currents have been developed. In these techniques the current conveyors are proved to be functionally flexible and versatile, rapidly gaining acceptance as a practical device with a wide range of high performance circuit and system applications. A host of circuits have been suggested on synthesis of various circuit elements using current conveyors.

In this paper, analog multiplier and divider circuit and also frequency divider is proposed using CCCII. A multiplier is an important component for the design of analog nonlinear function circuits. An analog multiplier is an important circuit for many applications such as adaptive filters and frequency modulators. And also it is found application in automatic gain control, frequency translation, waveform generation, linear modulation, neural networks, and other signal processing circuits.

The introduced amplitude multiplier/divider and frequency divider configuration can be realized by n-p-n and p-n-p transistors to easily accomplish its experimental test. PSPICE simulation is used to verify the performance of circuit design and to predict the circuit behavior. SPICE (simulation program for integrated circuit emphasis) is a general purpose analog circuit simulator.

II. DESCRIPTION OF THE CCCII+

The current controlled conveyor is a three-terminal device with two input terminals X & Y and an output terminal Z with unity gain. The second generation current controlled conveyor (CCCII) which implemented with the BJT by Fabre in 1995.

One of the reasons we use second generation current controlled conveyor (CCCII) is that it allows implementation of electronic functions usable at high frequency.

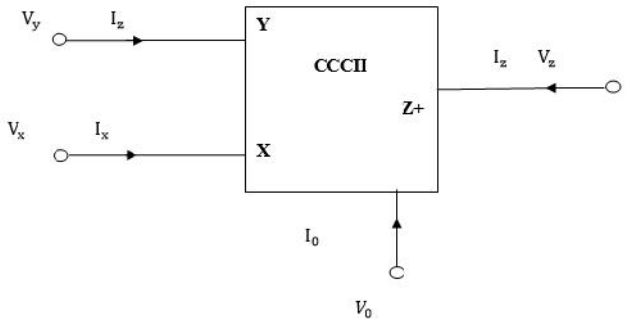

Fig.1: Electrical symbol of the CCCII+.

A second generation Current Controlled Conveyor (CCCII) is characterized by $I_y = -0, V_x = V_y + I_x R_x, I_z = \pm I_x$, and its matrix form is shown below

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

Using the standard notation for the CCCII+, whose electrical symbol is shown in Fig.1.

III. PROPOSED CIRCUIT

The internal structure of CCCII+ is constructed with ±2.5V symmetrical dc power supply voltages. The p-n-p and n-p-n transistors are used to implement the CCCII+ is simulated by using SPICE which is shown in fig.2.

The intrinsic resistance of the CCCII+ is defined as

$R_x = V_T / 2I_0$ (2)

Multiplication is intended to perform a linear product of two continuous signals and, yielding an output equation given by

The total output current of realized circuit for multiplier is

$$I_{out} = \frac{i1i2}{8I} \quad (3)$$

Block diagram of multiplication/divider, it can perform a four quadrant multiplication if the input signals are i_1 and i_2, while it realizes a divider circuit the total output current of divider is

$$I_{out} = \frac{i1i2}{I} (4)$$

CIRCUIT DESCRIPTION OF CASCADED MULTIPLIER /DIVIDER

We also perform the multiplier/divider in which CCCII+ building block is connected in cascaded form. The proposed analog multiplier/divider circuit which is connected in cascaded is shown in fig.3.

The intrinsic resistance of the CCCII+ (first block) is defined as

$$R_{x1} = V_T / 2 (I_0 + i_2) \quad (5)$$

The intrinsic resistance of the CCCII+ (second block) is defined as

$$R_{x2} = V_T / 2I \quad (6)$$

Multiplication is intended to perform a linear product of two continuous signals and, yielding an output equation given by

The total output current of realized circuit is

$$I_{out} = i_1 (1 - R_{x1}/R_{x2}) \quad (7)$$

By substituting eq.5 and eq.6 in eq.7, yields

$$I_{out} = \frac{i1i2}{I} \quad (8)$$

Block diagram of cascaded multiplication/divider, it can perform also a four quadrant multiplication if the input signals are i_1 and i_2, while it realizes a divider circuit if the input signals are i_1 (or i_2) and I.

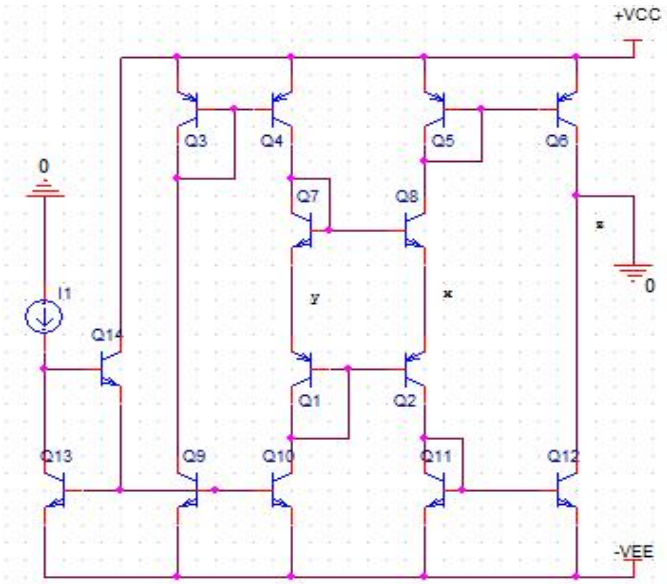

Fig.2: Internal structure of the CCCII+ based on BJTs.

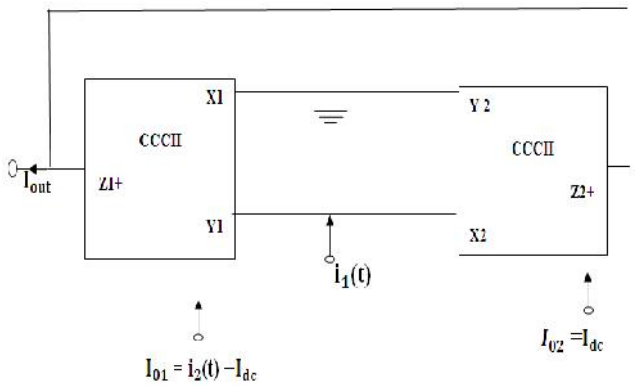

Fig.3: Block diagram of Multiplication/Divider.

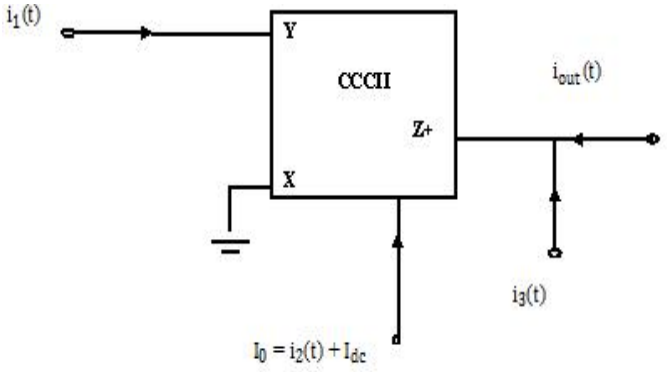

Fig.4: proposed multiplier/divider circuit.

IV. SIMULATION RESULTS

Case1: Two-quadrant multipliersimulation results are given in Fig.6, where a 25-μA peak sinusoidal current at 100 kHz is multiplied by a 25-μA dc current. In other words,$i_1(t)$= 25 μA sin (2π ×10^5t), I_0= 25 μA, and $i_3(t)=i_2(t)$ =0 are chosen to achieve two-quadrant multiplication.

Case2: The multipliersimulation results are given in Fig.7, where $i_1(t)$= 100μA sin (2π × 8x10^5t), I_0= 5μA + 100μA sin(2π x 10^6t) and $i_2(t)=i_3(t)$ =0 are selected for four-quadrant multiplication.

Case3: The divider function simulation results are given by fig.9, where i_1=80μA as a triangular signal withperiod =2ms and I as a triangular signal with amplitude 20μA, DC component =50μA and period =2ms.

Case4:Frequency-doublersimulation results are given in Fig.10, in which frequency doubling is achieved using two CM signals at 1000 kHz. That is, $i_1(t)$ = 22 μA sin (2π ×10^6t), I_o= 1 μA, and $i_3(t)$ = −22 μA sin (2π × 2x 10^6t) are selected for frequency Doubling.

Case5: The multiplier function simulation results are given by fig.11, where i_1 =1sin(2π1000t)mA, i_2 = 1sin(2π30000t)mA and I=2mA.

Case6: The divider function simulation results are given by fig.12, where i_1=20μA, i_2=100μA and I as a triangular signal with amplitude 10μA, DC component =20μA and period =2ms.

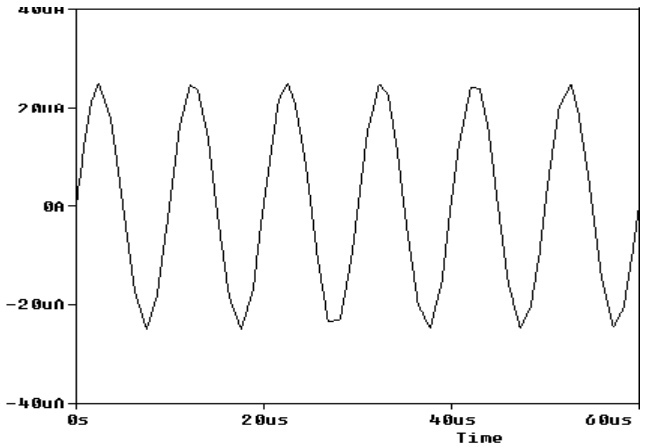

Fig.5: Input sinusoidal signal.

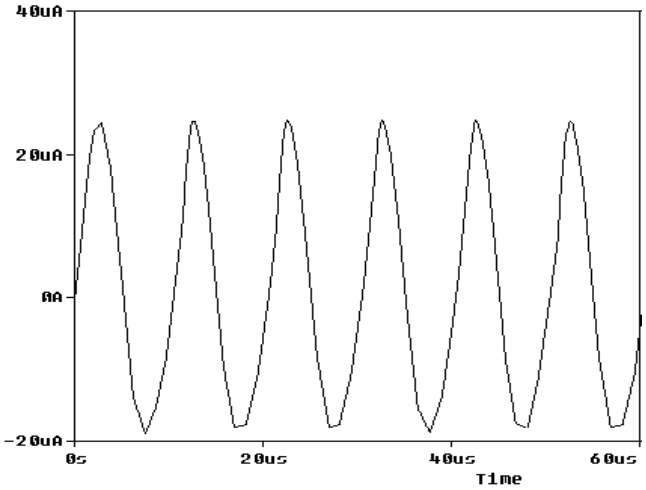

Fig.6: Two quadrant multiplication (case 1).

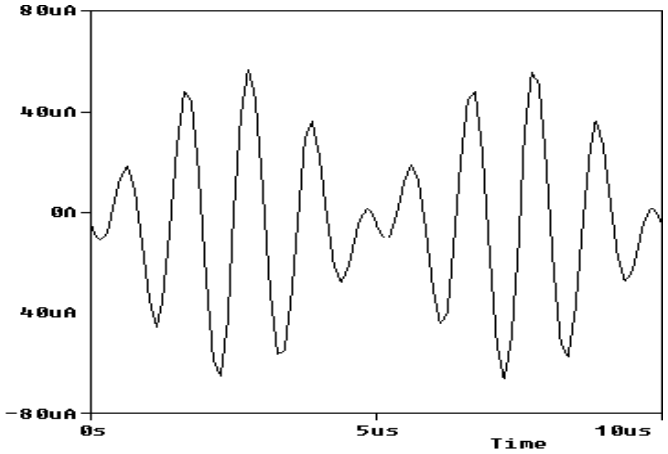

Fig.7: Multiplication output (case 2).

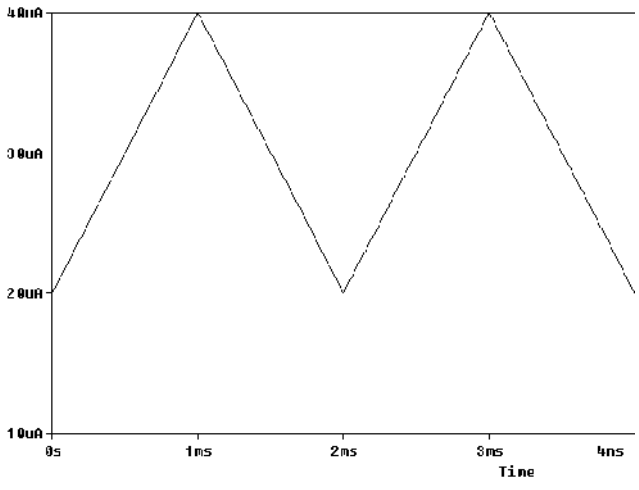

Fig.8: Divider input.

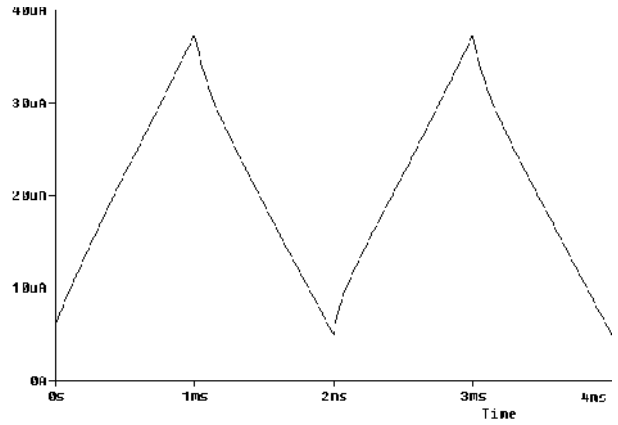

Figure 9: Divider output (case 3).

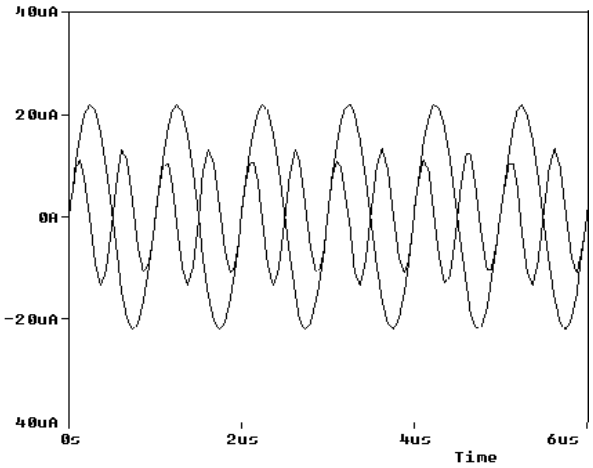

Figure 10: Frequency doubling output (case 4).

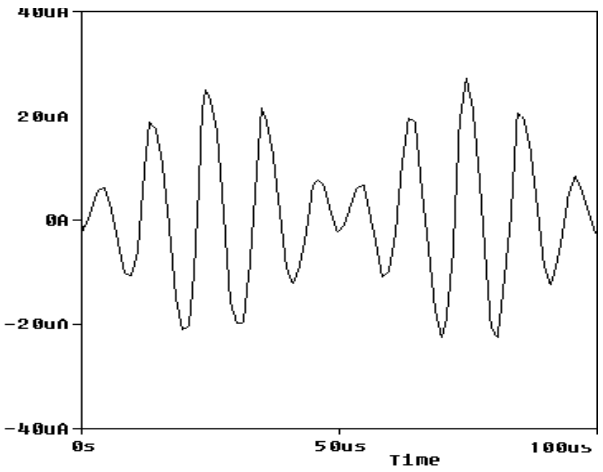

Fig.11: Multiplication output (case 5).

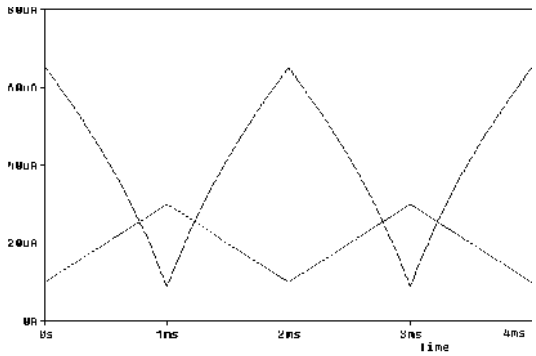

Figure 12: Divider input and output (case 6).

CONCLUSION

The proposed circuit performs analog multiplication/division using two current controlled current conveyors without any passive components. Without modifying the circuit of single CCCII+ it can perform current follower, four quadrant multiplication and frequency doubling. The circuit is implemented using Q2N4920 PNP and Q2N4921 NPN transistors with the 0.35 specifications. The simulation results are verified with theoretical results using PSPICE. The proposed multiplier/divider circuit is best suited for monolithic chip for use in battery powered, portable electronic equipment's such as wireless communication system devices or portable devices.

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